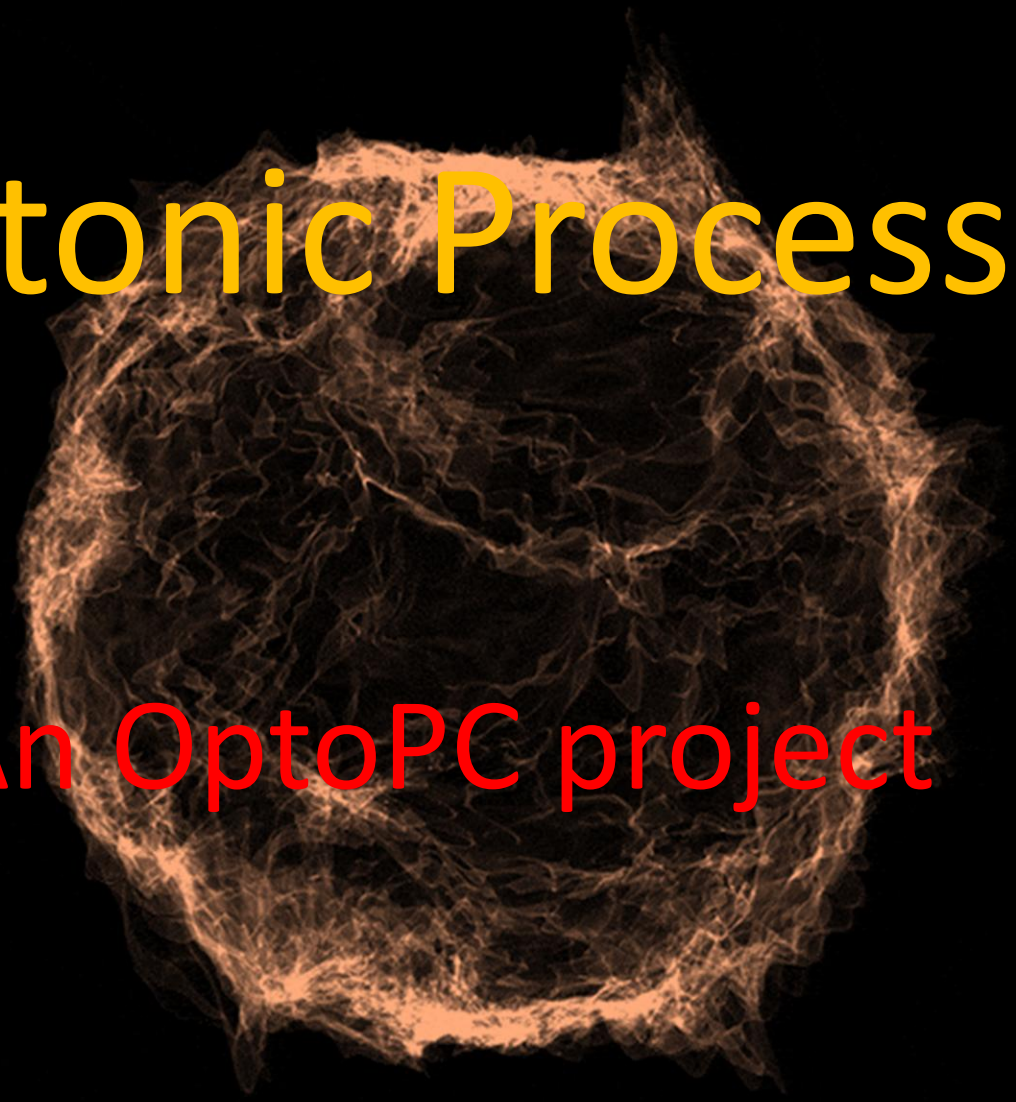
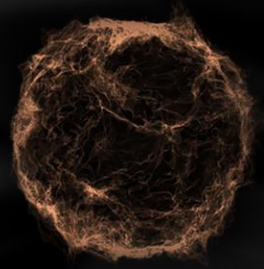
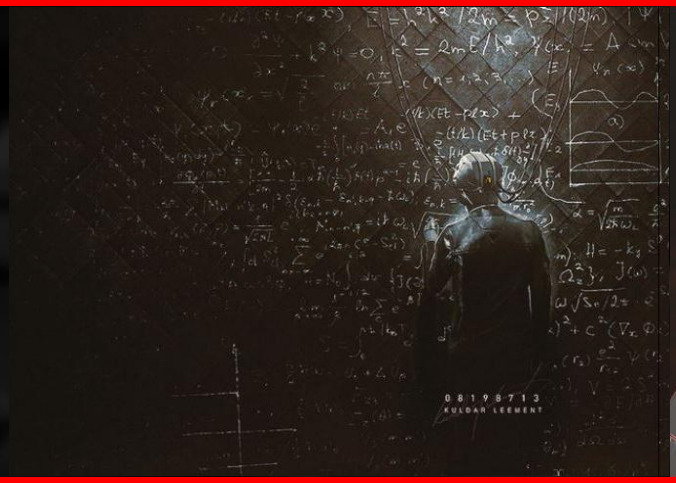
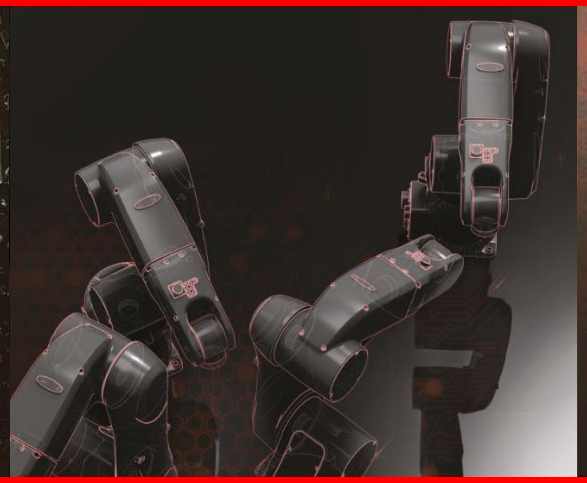
Photonic Processor



An OptoPC project




OptoPC project

Parallel Optical Computing System

REBEL DYNAMICS®

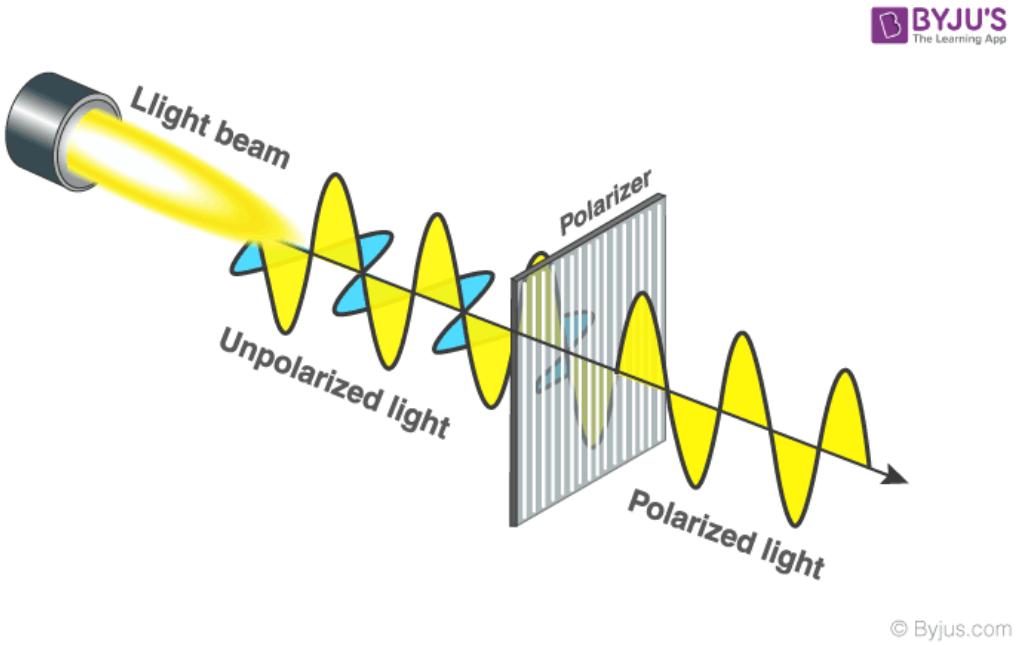
The project

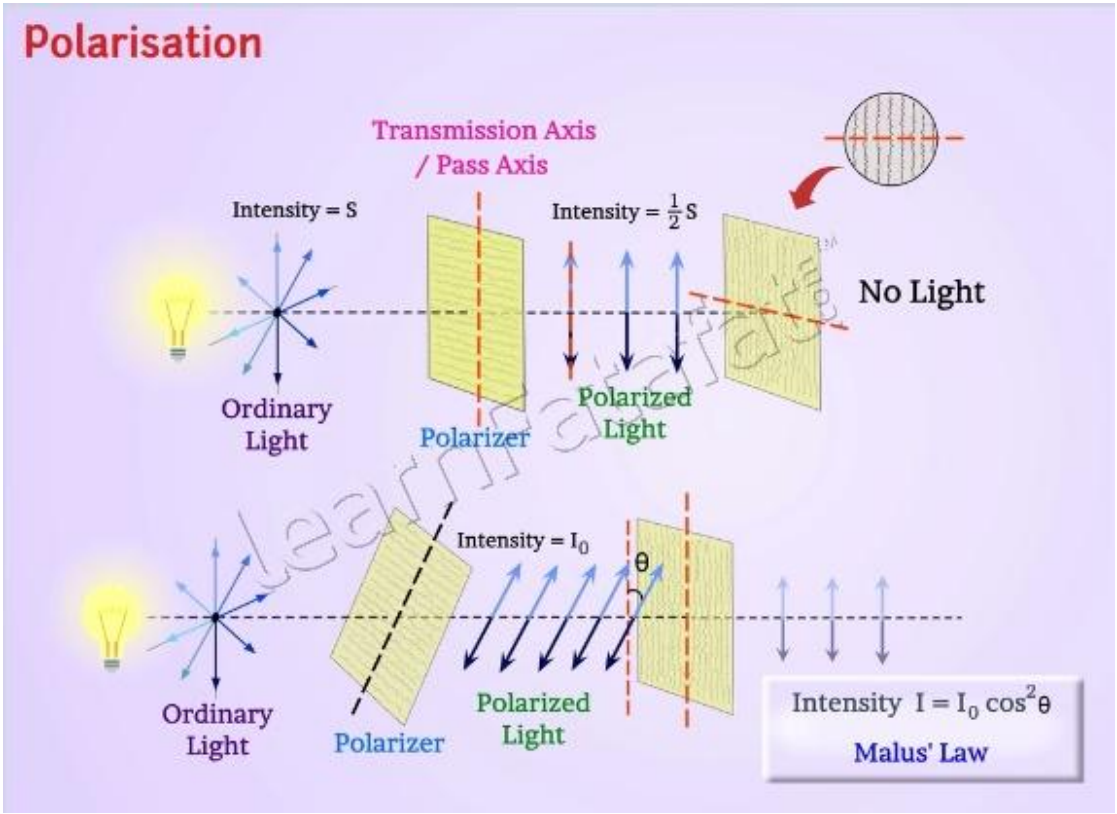


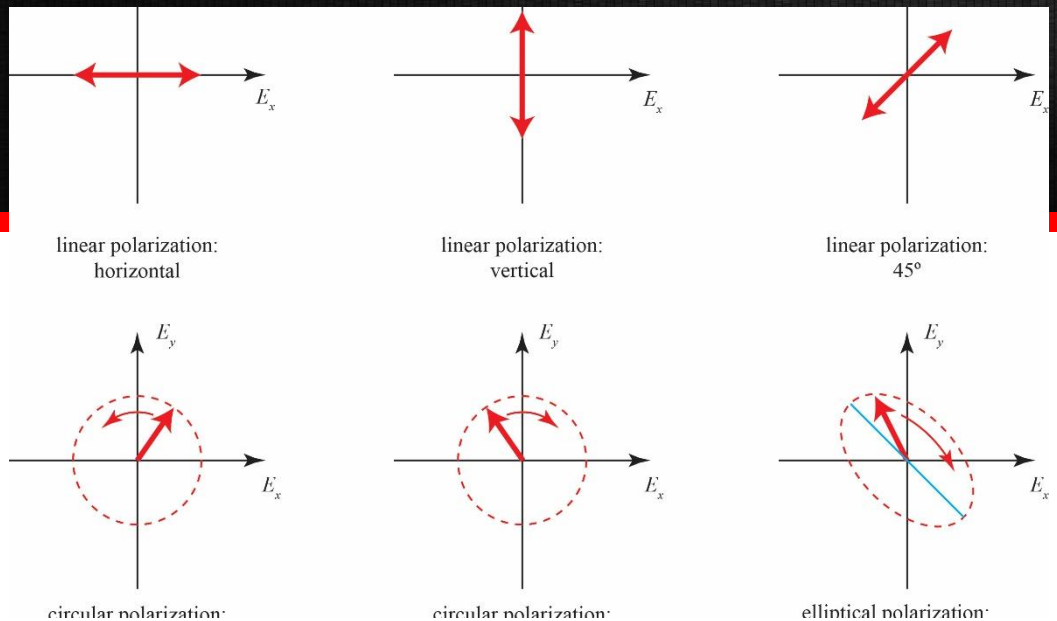
Photonic processor key Features

- Use light as Information carrier
- Use LCD as information modifier (Spatal Light Modulator)
- Very High parallelism
- Very low power consumption
- No thermal dissipation
- No fans, no cooling,no acoustic and thermal noise.
- Ideal for Carbon foot print

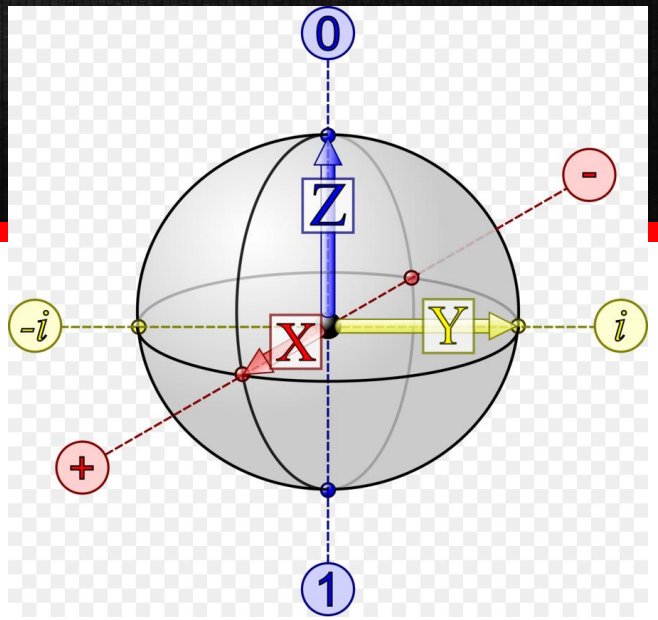
Photonic phisics

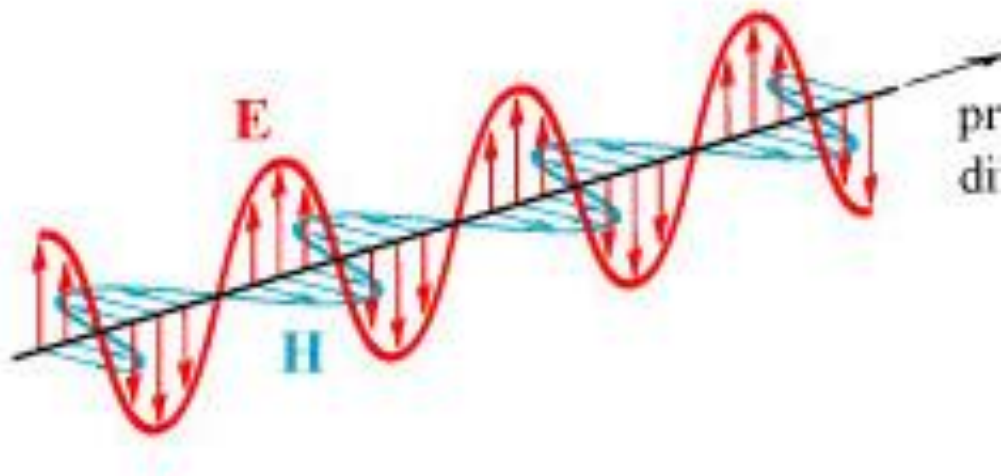


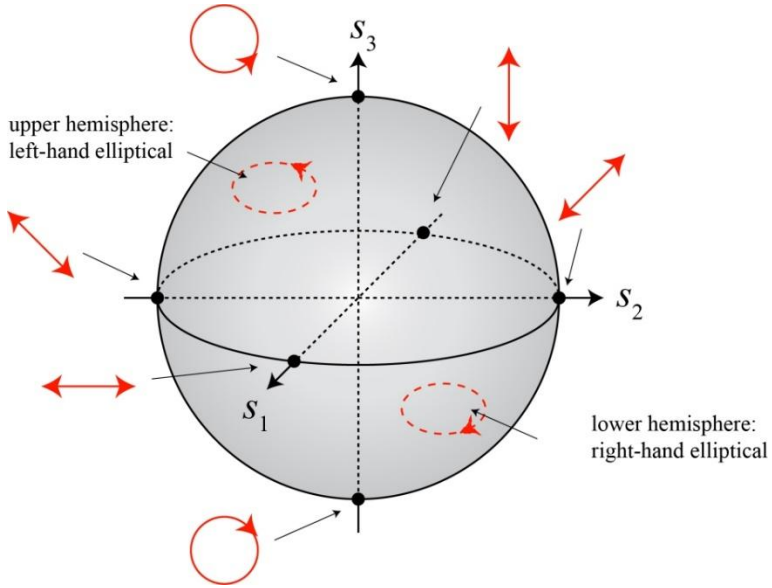




Photonic phisics

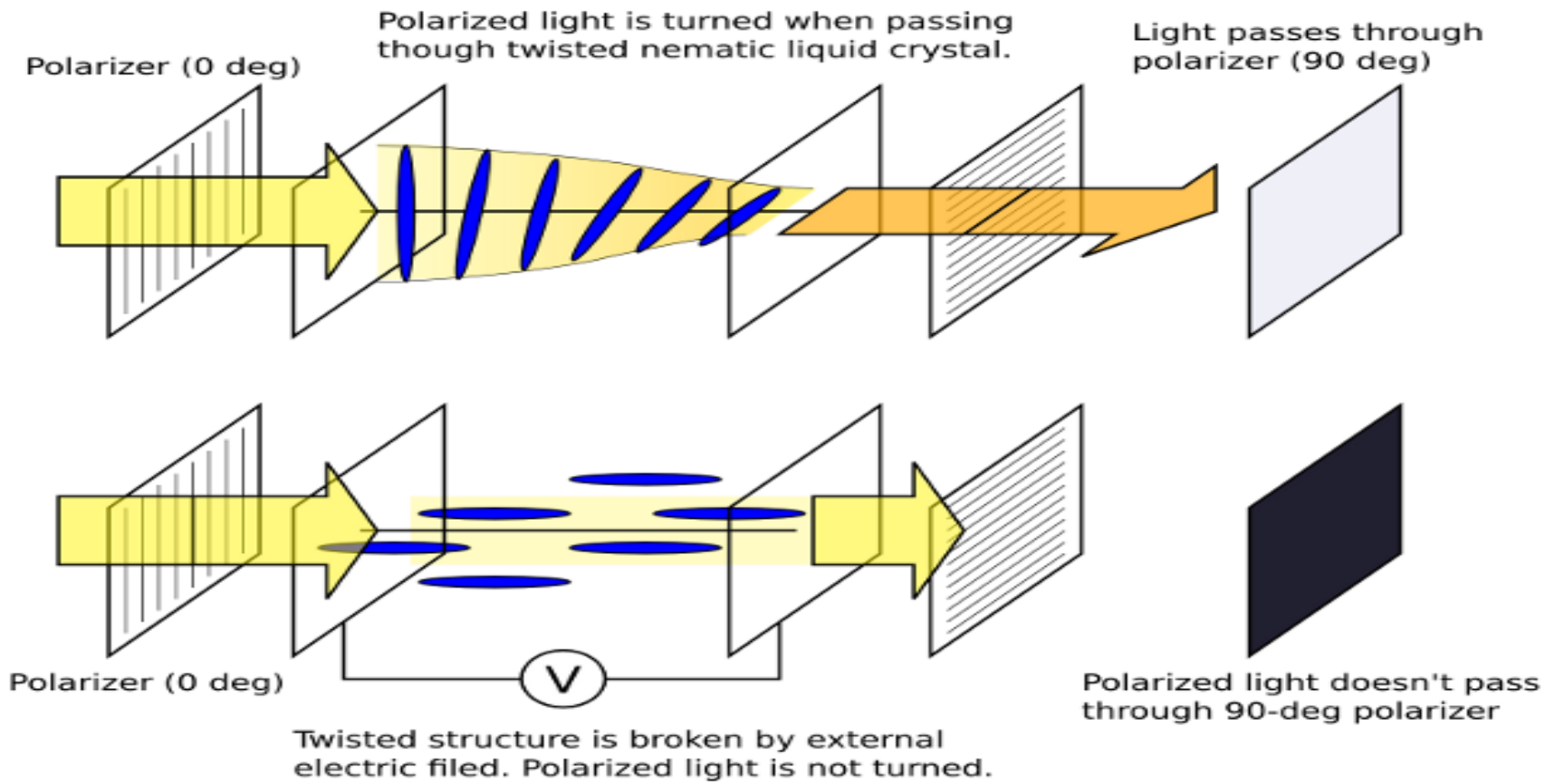


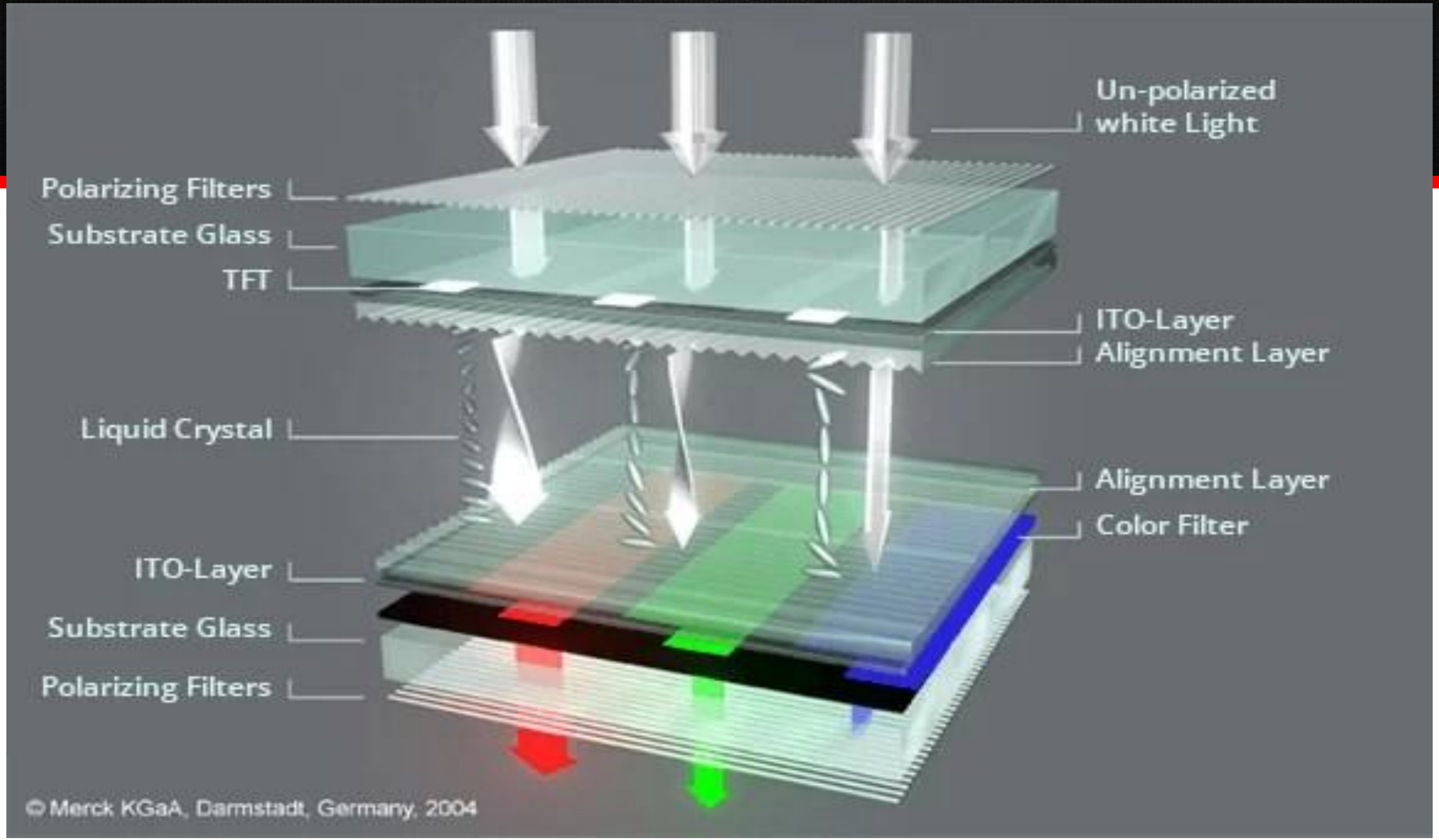


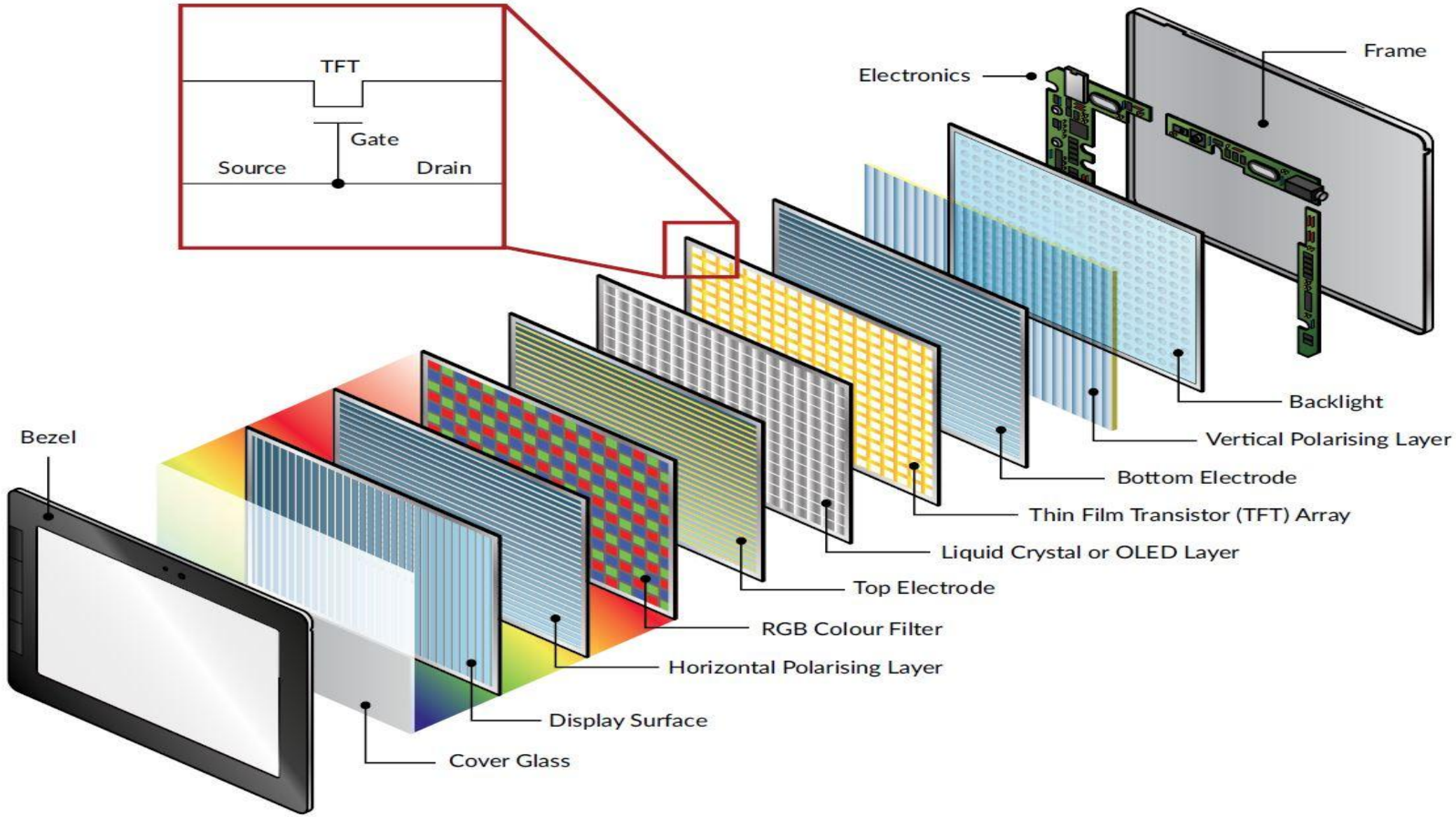


LCD

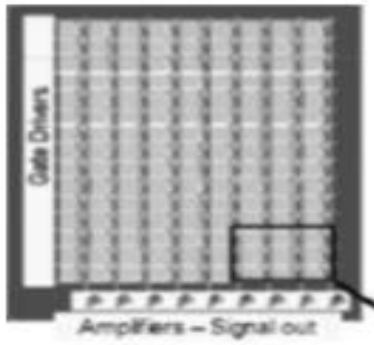
How LCD work s as phase shifter




Un-polarized
white Light
Polarizing Filters
Substrate Glass
TFT
ITO-Layer
Alignment Layer
Liquid Crystal
Alignment Layer
Color Filter
ITO-Layer
Substrate Glass
Polarizing Filters
© Merck KGaA, Darmstadt, Germany, 2004

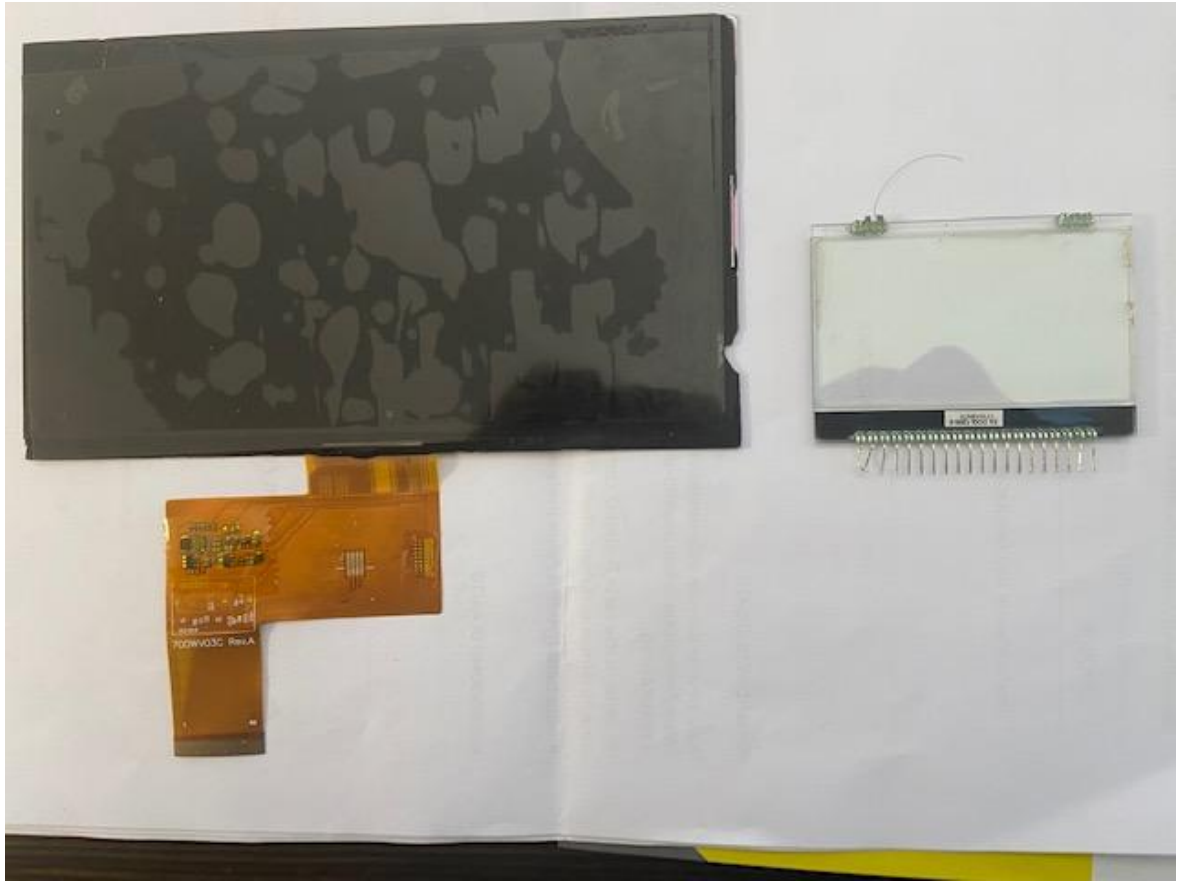

TFT
Gate
Source
Drain
Electronics
Frame
Backlight
Vertical Polarising Layer
Bottom Electrode
Thin Film Transistor (TFT) Array
Liquid Crystal or OLED Layer
Top Electrode
RGB Colour Filter
Horizontal Polarising Layer
Display Surface
Cover Glass
Bezel

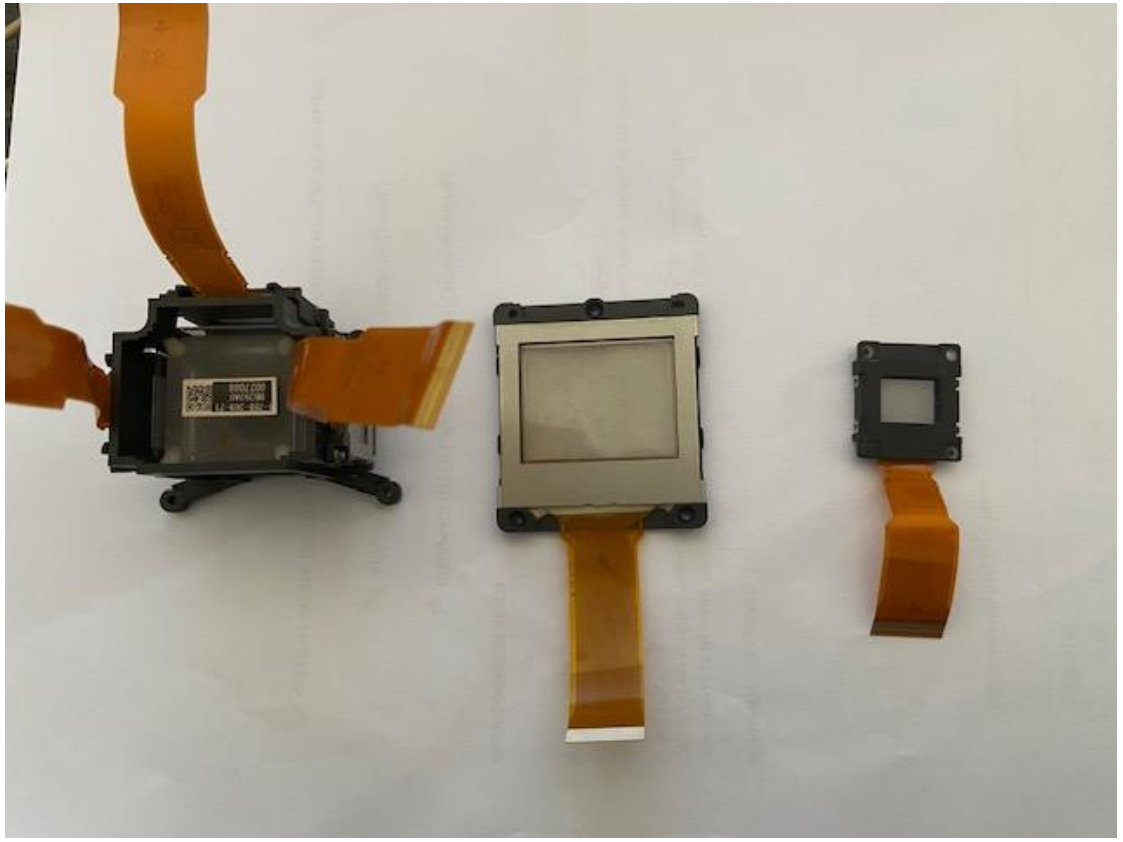
TFT *active matrix* array
(Amorphous Silicon)



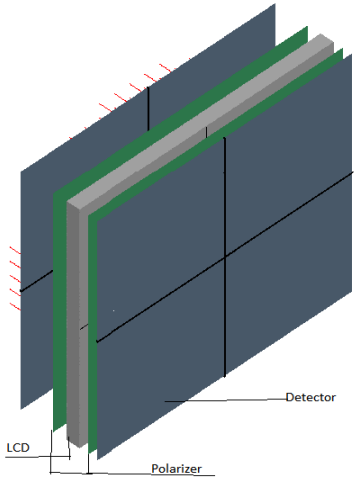
Gate switches
G1
Active Area
Thin-Film Transistor
Dead Zone
G2
Storage Capacitor
G3
Charge Collector Electrode
D1
D2
D3
CR1
CR2
CR3
Data lines
Charge Amplifiers
Analog to Digital Converters

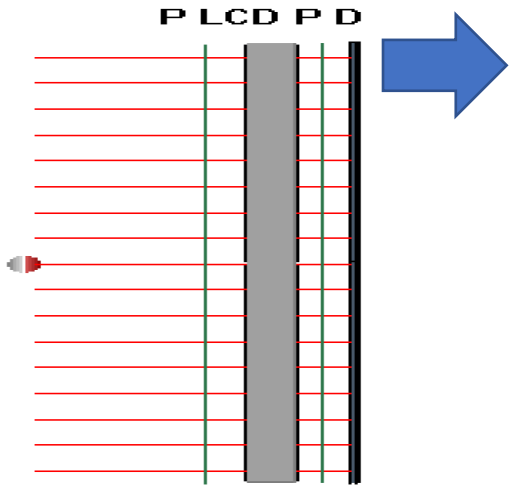
Testing and prototyping

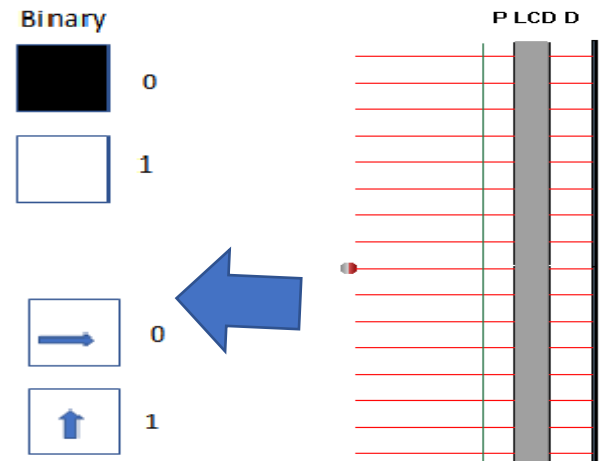


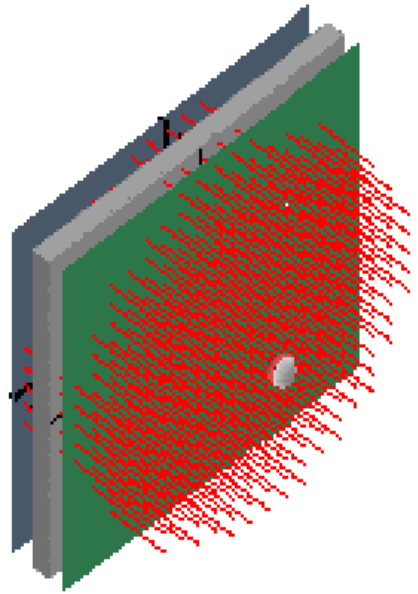


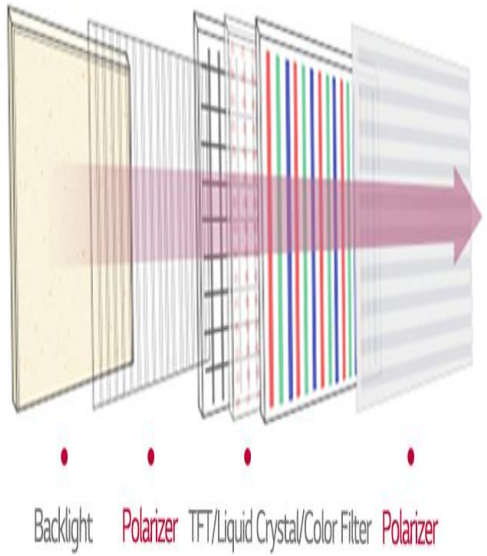
Binary coding

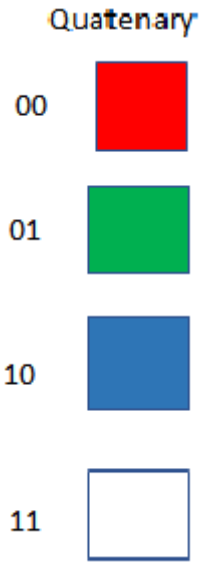








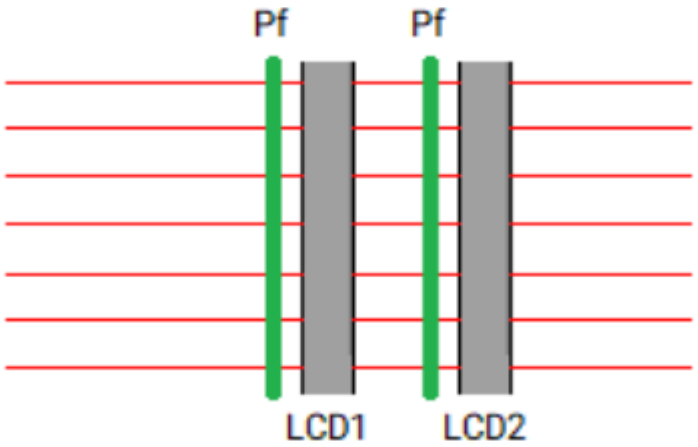




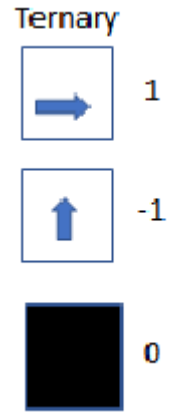
LG Display Newsroom

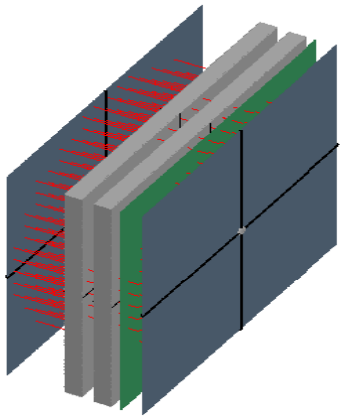
LCD can manipulate millions rays
In parallel and each ray
Can have 2,3.4……32 symbols

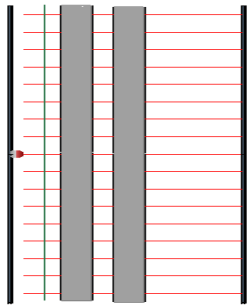
Adding a second LCD means manipulate data out

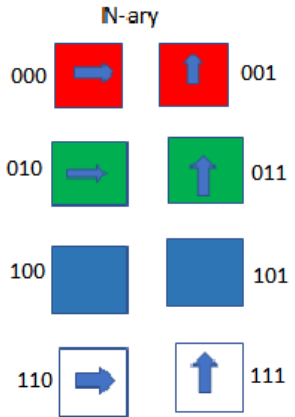


Pf	LCD1	Pf	LCD2	out
V	0	V	0	V
V	0	V	1	H
V	1	V	0	Black
V	1	V	1	Black

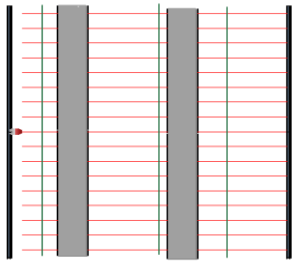








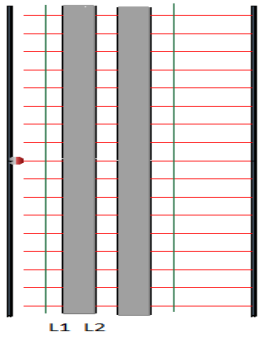
With two LCD we can make logic gates



AND gate
Incoming V pol light
Is detectd (1) only if the 2 Lcd
Are in 1 state (inactive)

LCD=0 active V->H H>V
LCD=1 inactive V->V H->H

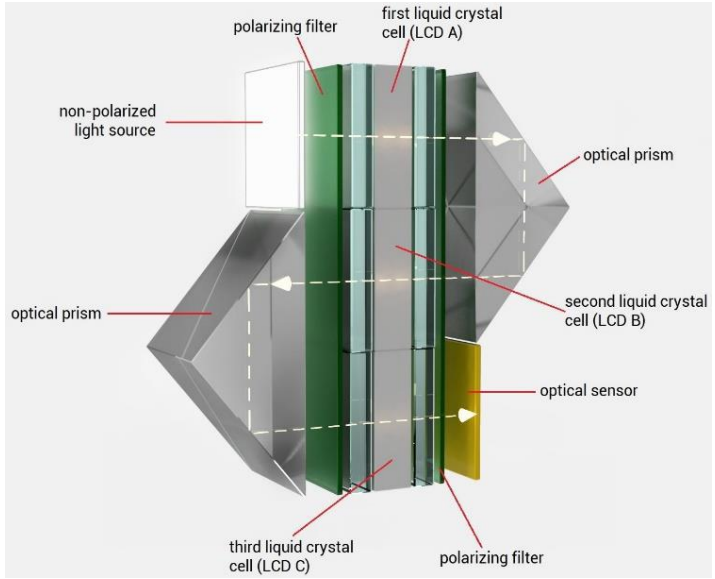
Pf	LCD1	Pf	LCD 2	out
V	0	V	0	0
V	0	V	1	0
V	1	V	0	0
V	1	V	1	1



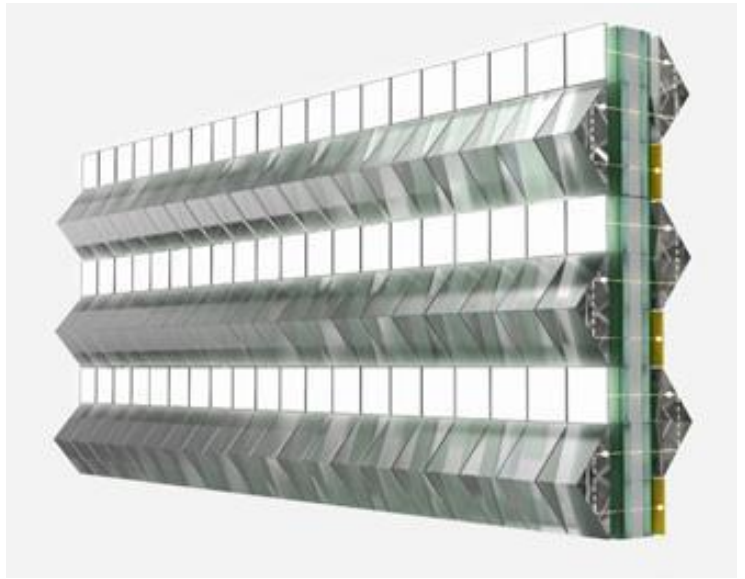
X-OR gate
Incoming V pol light
Is detected) (1) only if
Both LCD are in the same state

Pf	LCD1	Pf	LCD 2	out
V	0	V	0	1
V	0	V	1	0
V	1	V	0	0
V	1	V	1	1

Processor device scheme

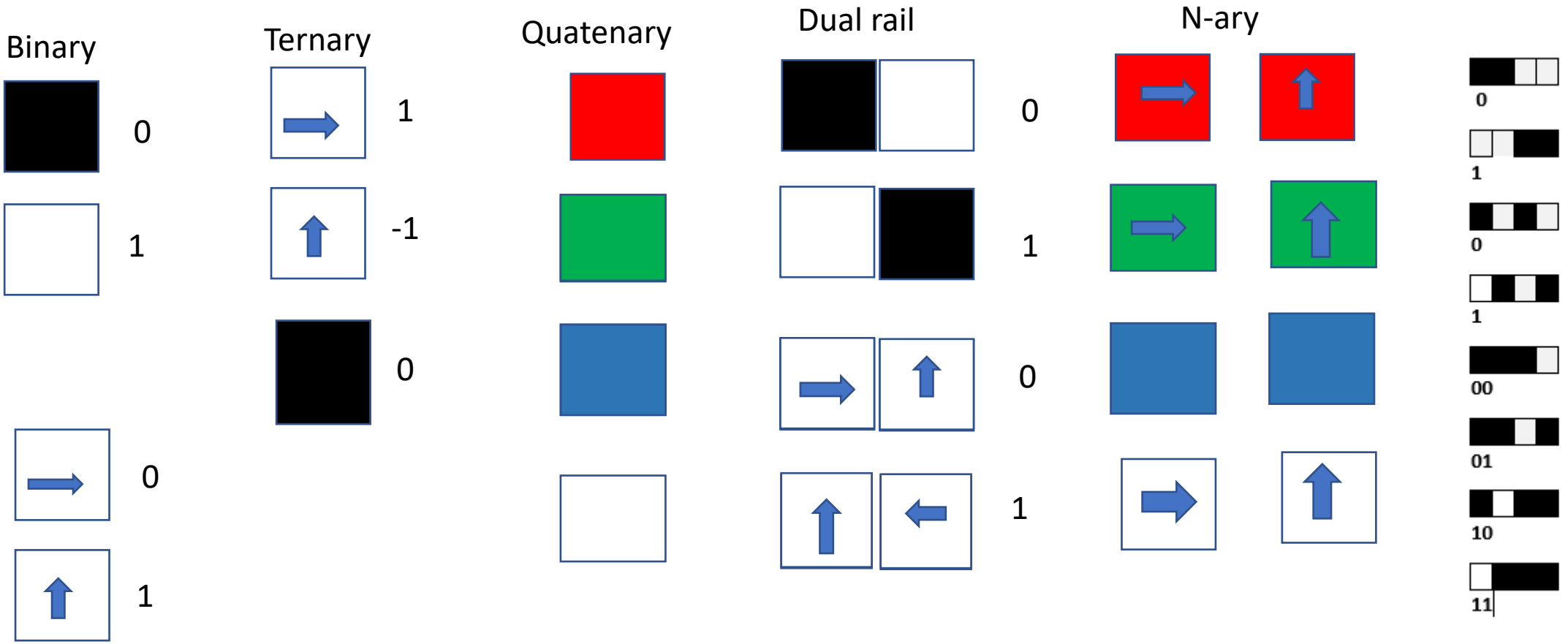


Single Optical-electronic element



Optical parallel computing device

How data is encoded for each pixel



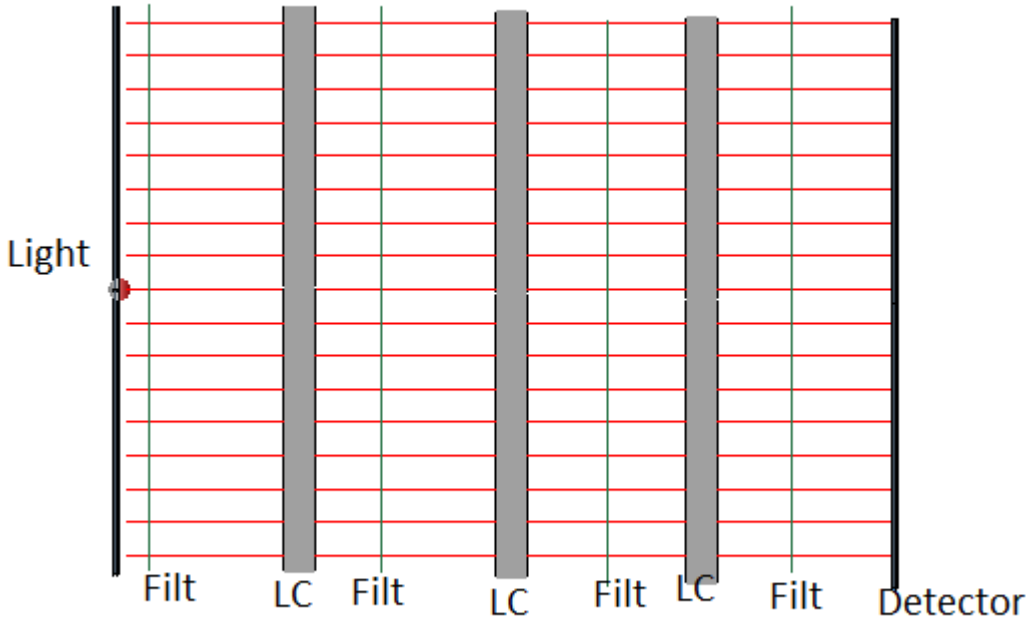
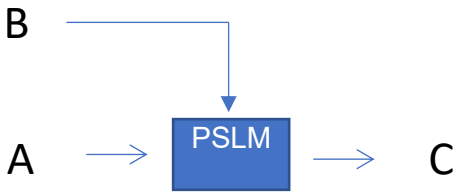
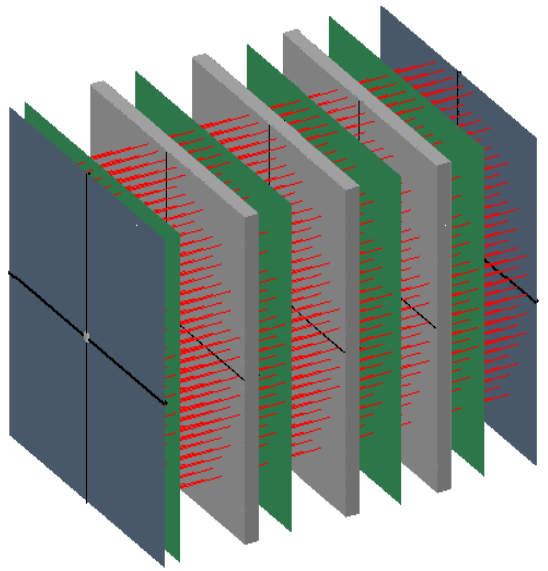


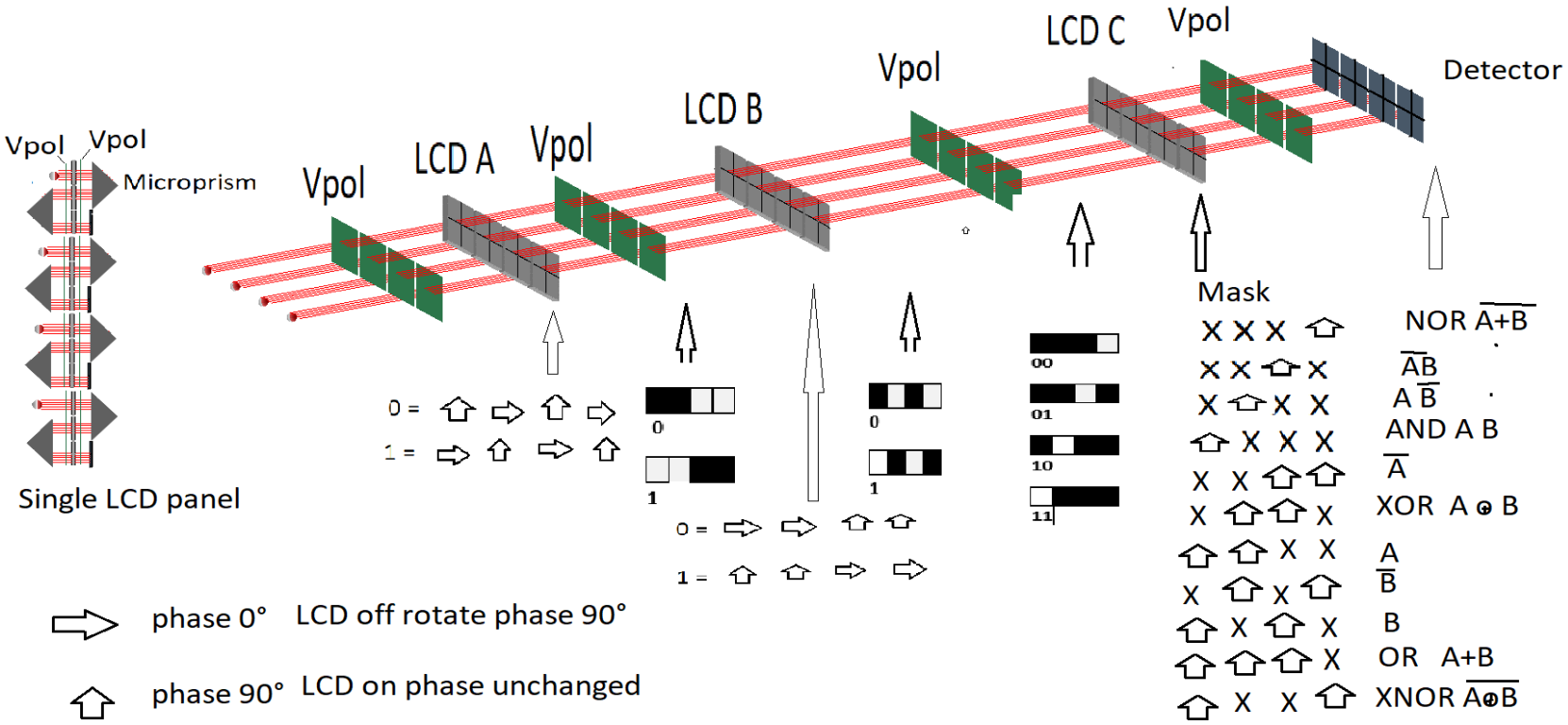
Tabella per ingresso Luce polarizzata Orizzontalmente

VALORI STATO MODULATORE					USCITA	TERNARY CODE
LCD3	Pol1	LCD4	Pol2	LCD5		
0	Vp	0	Hp	0	V	1
0	Vp	0	Hp	1	H	-1
0	Vp	1	Hp	0	W	0
0	Vp	1	Hp	1	W	0
1	Vp	0	Hp	0	W	0
1	Vp	0	Hp	1	W	0
1	Vp	1	Hp	0	W	0
1	Vp	1	Hp	1	W	0





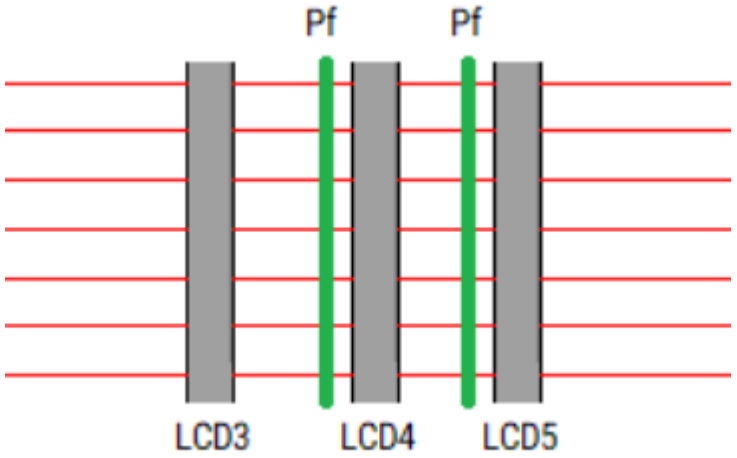
Logic operation



Example of Logic operation using dual rail coding

LCD Control Logic Unit

- Logic operation



a	b	U	LC3	LC4	LC5
H	H	H	0	1	0
H	V	V	0	1	1
V	H	V	1	1	1
V	V	W	1	0	0

a b	r
0 0	0
0 1	1
1 0	1
1 1	2

11011 + 27+

11010= 26=

22021 53

OptoPC



OptoPC Data Flow

- **Binary computer use 2 symbol per digit 0 1**
- **Arithmetic operation speed is limited by the «carry problem» and are intrisecally sequential**
- **Optical encoding increase the symbol per digit and ere free of «carry» using RNS (redundant Number system) algorithm**
- **Parallelism of millioms of optical symbol**
- **Multivalue logic**



Some Number system applied in optical computing

- Negabinary Number system
- RNS Redundant number system
- MSD modified Signed Digit
- Modular Aritmetic
- Residuenumber System
- Ternary number System

RB - REDUNDANT BINARY NUMBER REPRESENTATION

G. A. De Biase, A. Massini “Redundant binary number representation for an inherently parallel arithmetic on optical computers”,

Appl. Opt., 32 (1993)

High efficiency redundant binary number representations for parallel arithmetic on optical computers

G. A. DE BIASE, A. MASSINI

A family of redundant binary number representations, obtained by generalization of the RB (redundant binary) number representation, is introduced. All these number representations are suitable for optical computing and have properties similar to the RB representation. In particular, the p-RB (packed redundant binary) number representation introduced in this work has efficiency greater than both RB and MSD (modified signed digit) representations. With p-RB numbers the algebraic sum is always permitted in constant time for any efficiency value. p-RB representations also fit in a natural way the 2's complement binary number system. Symbolic substitution truth tables for the algebraic sum and several examples of computation are also given.

KEYWORDS: optical computing, redundant number representations, redundant binary numbers, parallel arithmetic units

Redundant number systems

Intensive Computation

Annalisa Massini

2017/2018

MODIFIED SIGNED DIGIT REPRESENTATION

A. K. Cherri, M. A. Karim, “Modified-signed digit arithmetic using an efficient symbolic substitution”, Appl. Opt. (1988)

Negabinary Number system

Parallel optical negabinary arithmetic based on logic operations

Guoqiang Li, Liren Liu, Lan Shao, Yaozu Yin, and Jiawen Hua

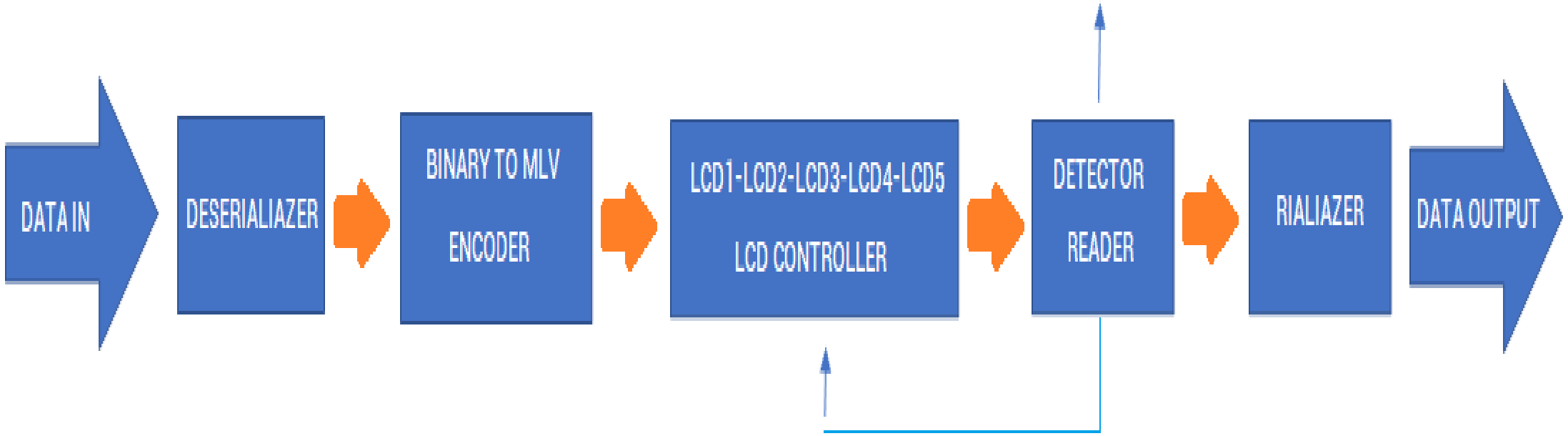
On the basis of signed-digit negabinary representation, parallel two-step addition and one-step subtraction can be performed for arbitrary-length negabinary operands. The arithmetic is realized by signed logic operations and optically implemented by spatial encoding and decoding techniques. The proposed algorithm and optical system are simple, reliable, and practicable, and they have the property of parallel processing of two-dimensional data. This leads to an efficient design for the optical arithmetic and logic unit. © 1997 Optical Society of America

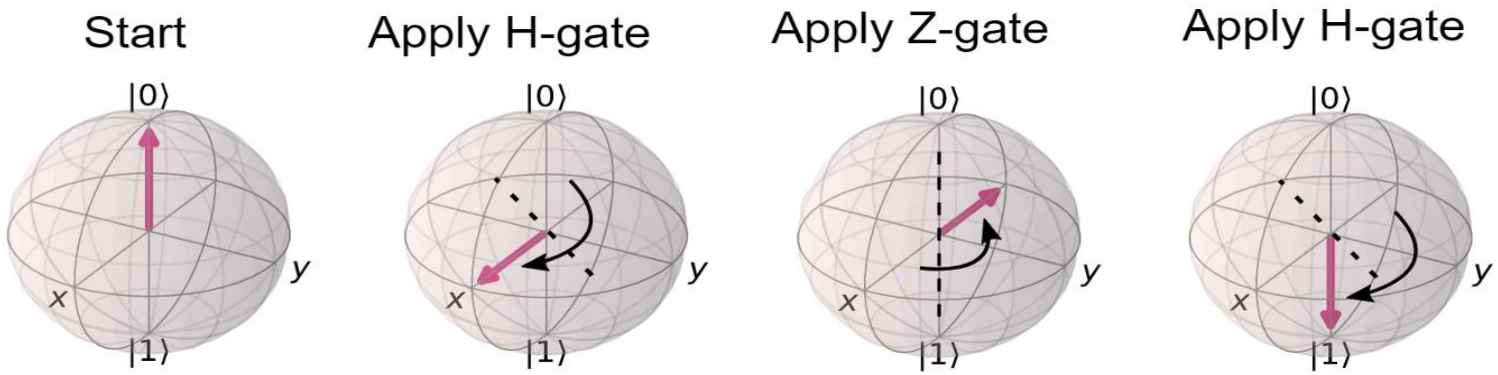
2. Parallel Negabinary Arithmetic Operations

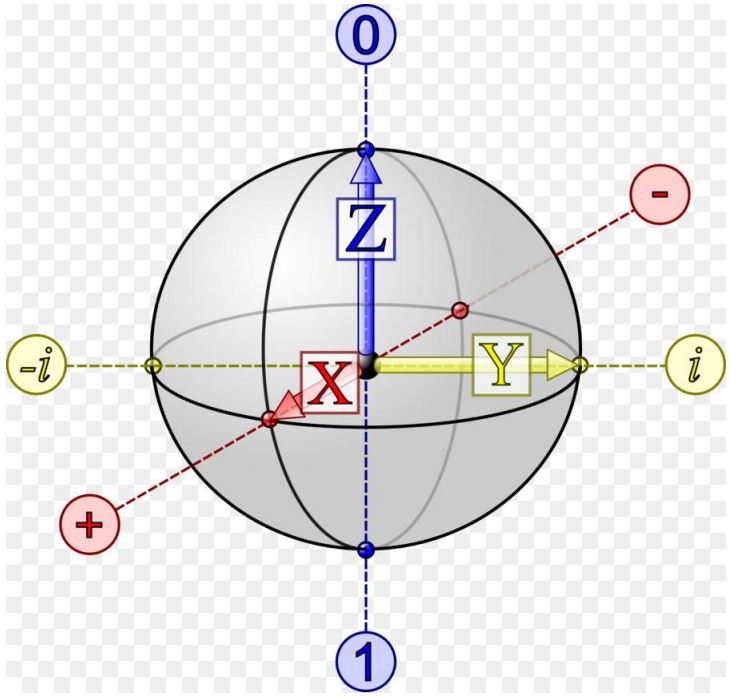
In the negabinary number system, a decimal number x has one and only one representation $x_{N-1} \ldots x_1 x_0 x_{-1} \ldots x_{-M}$, taking the form

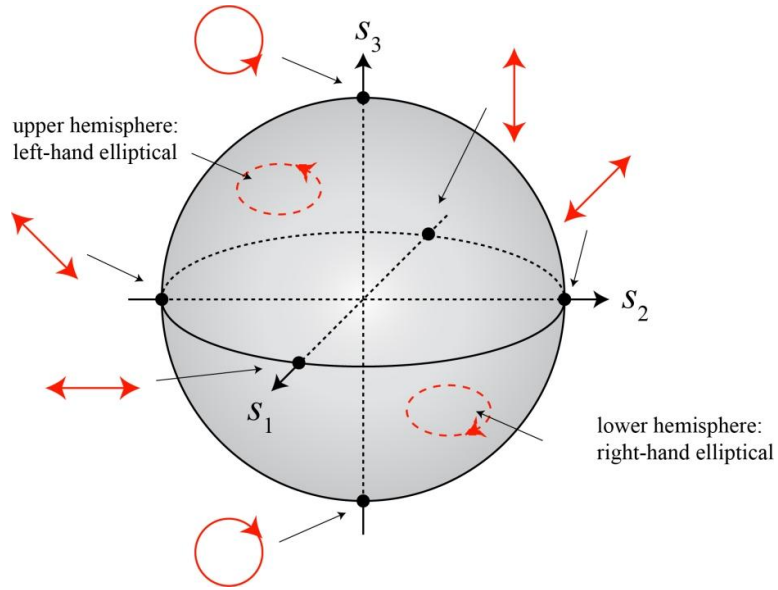
$$x = \sum_{i=-M}^{N-1} x_i (-2)^i, \qquad x_i \in \{0, 1\}, \tag{1}$$

LCD Control Logic Unit



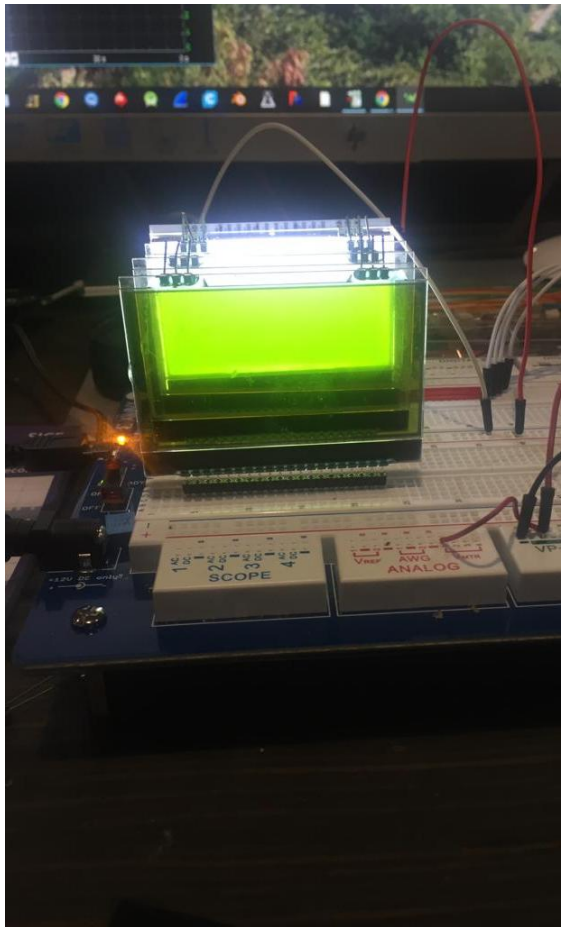

Start
Apply H-gate
Apply Z-gate
Apply H-gate
|0⟩
|1⟩
x
y

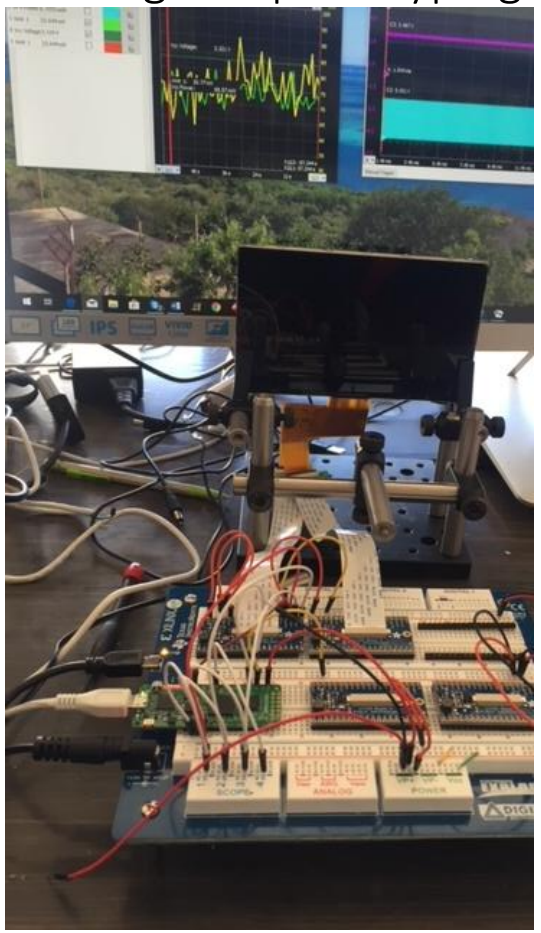

0
1
Z
X
Y
-
+
-i
i

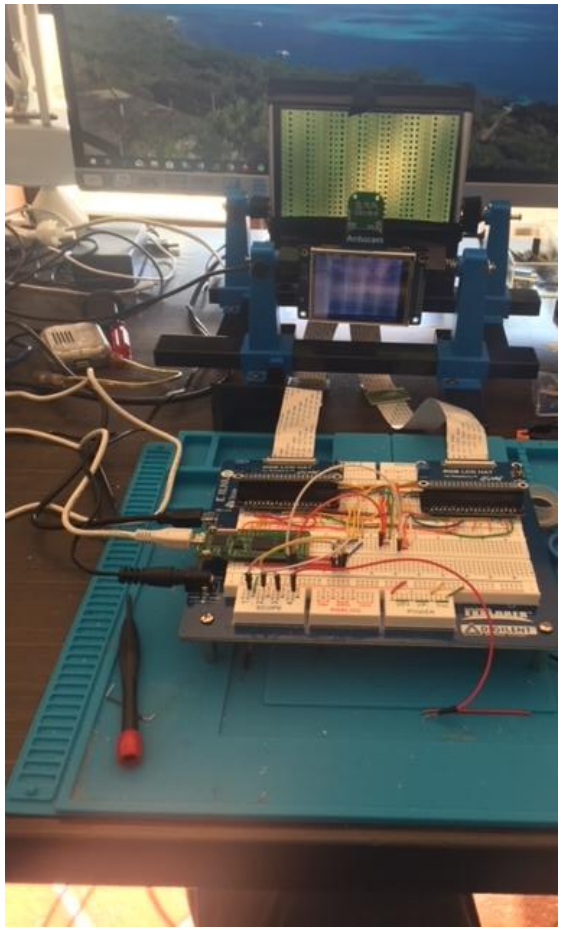

S_3
S_2
S_1
upper hemisphere:
left-hand elliptical
lower hemisphere:
right-hand elliptical

feasibility study

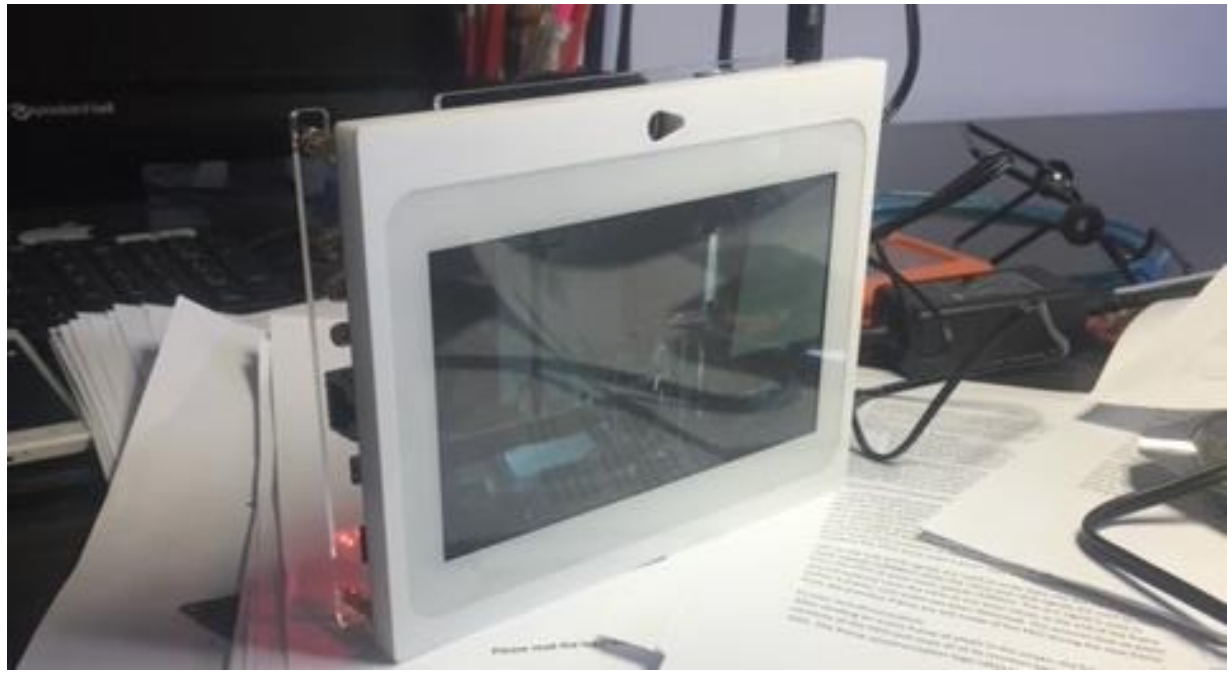
Testing and prototyping

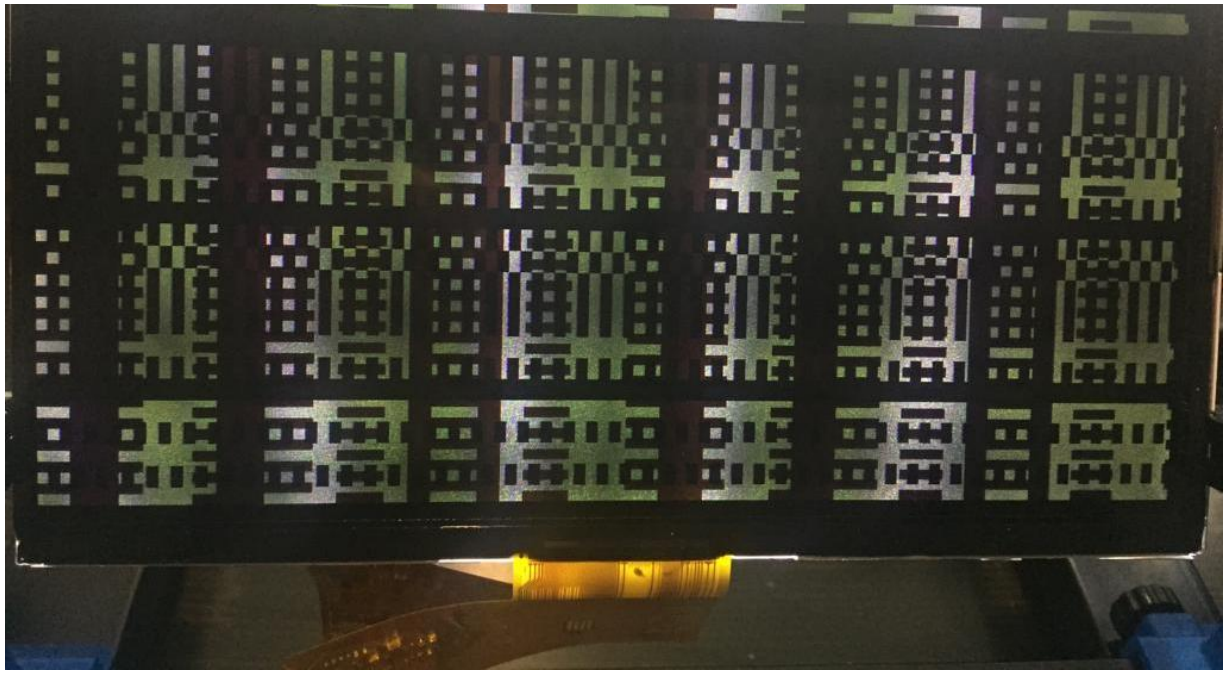




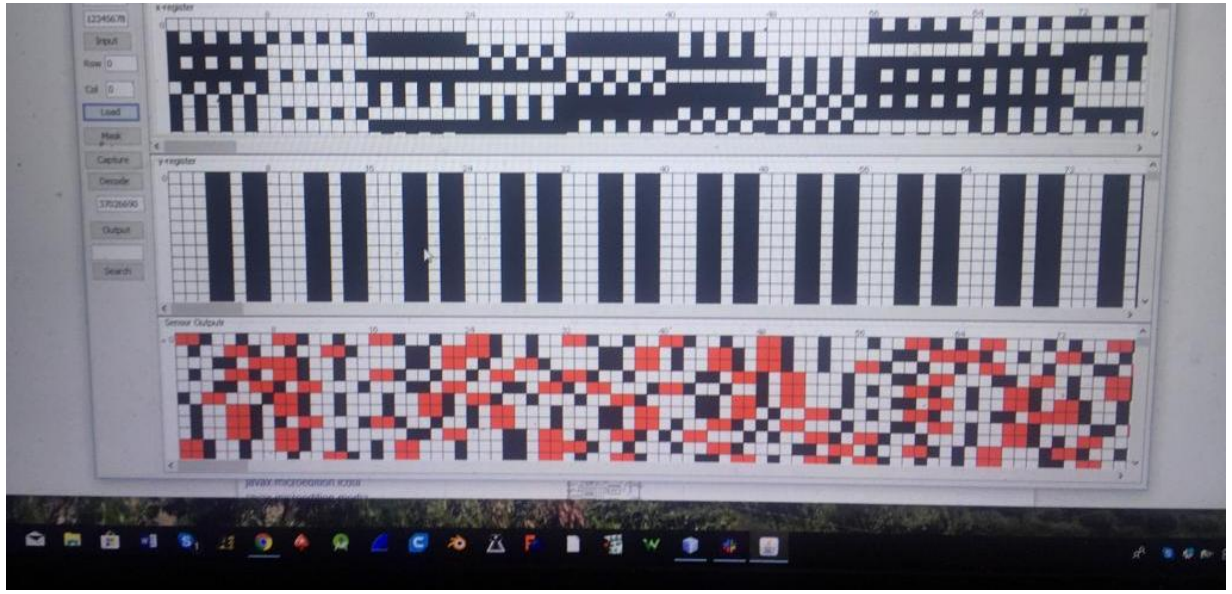


Testing and prototyping





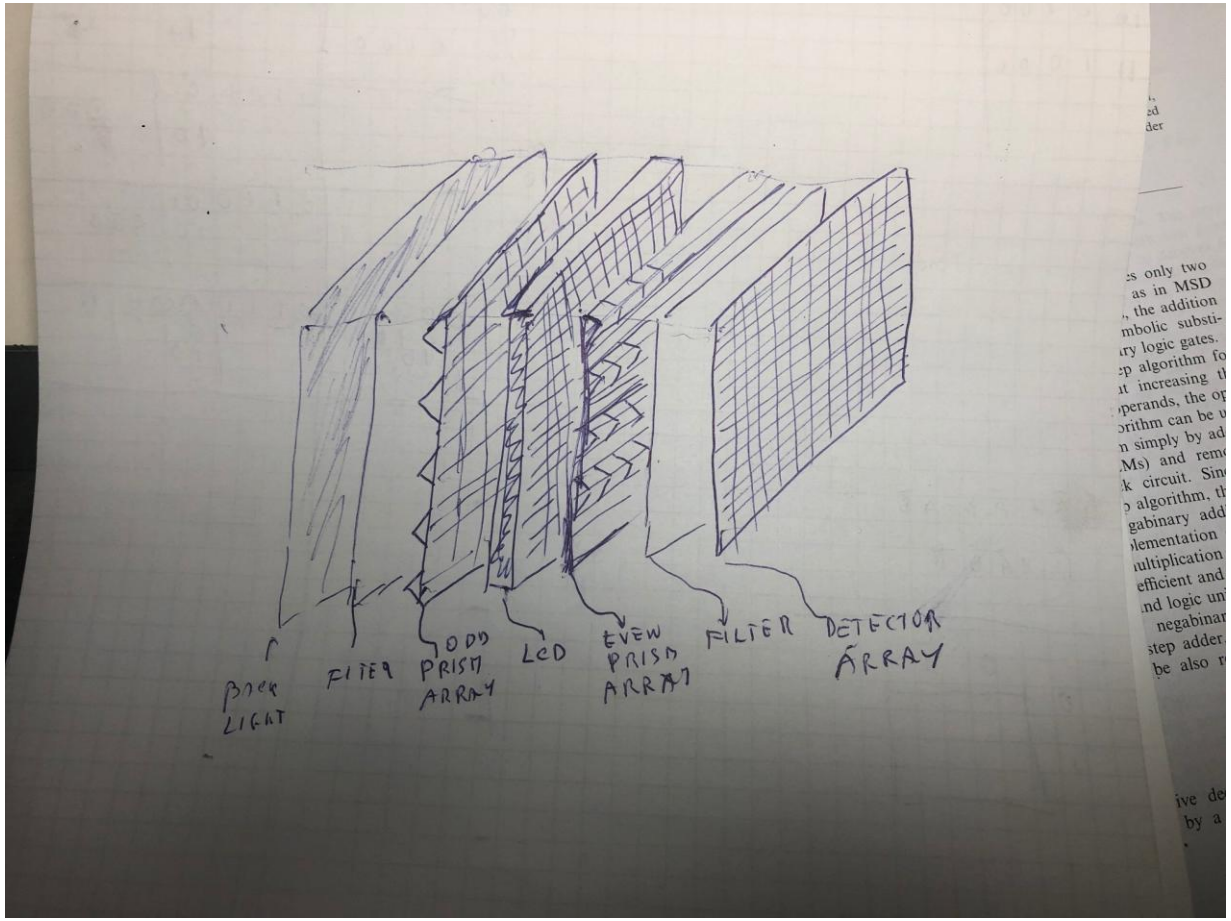
Testing and prototyping



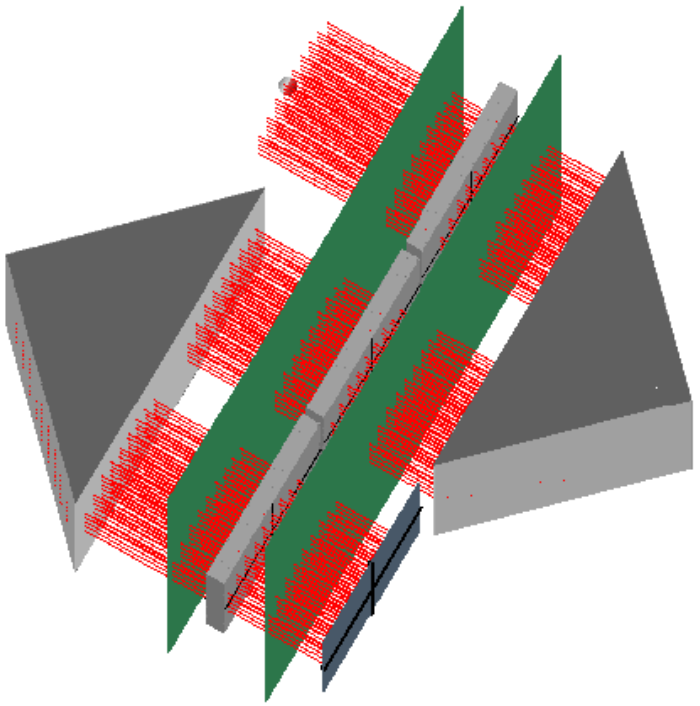


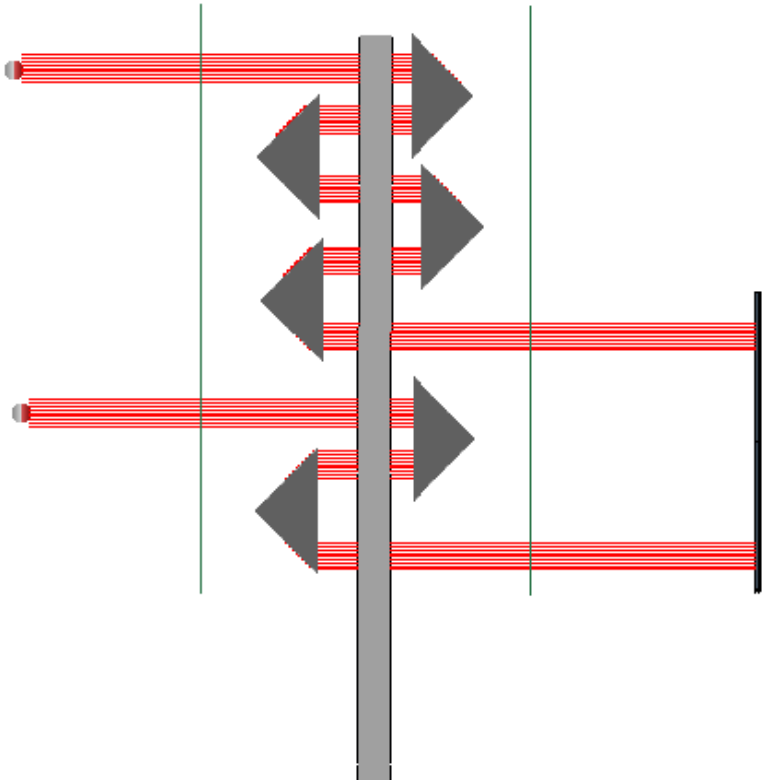
the concept

The first step



The first step





Simulation

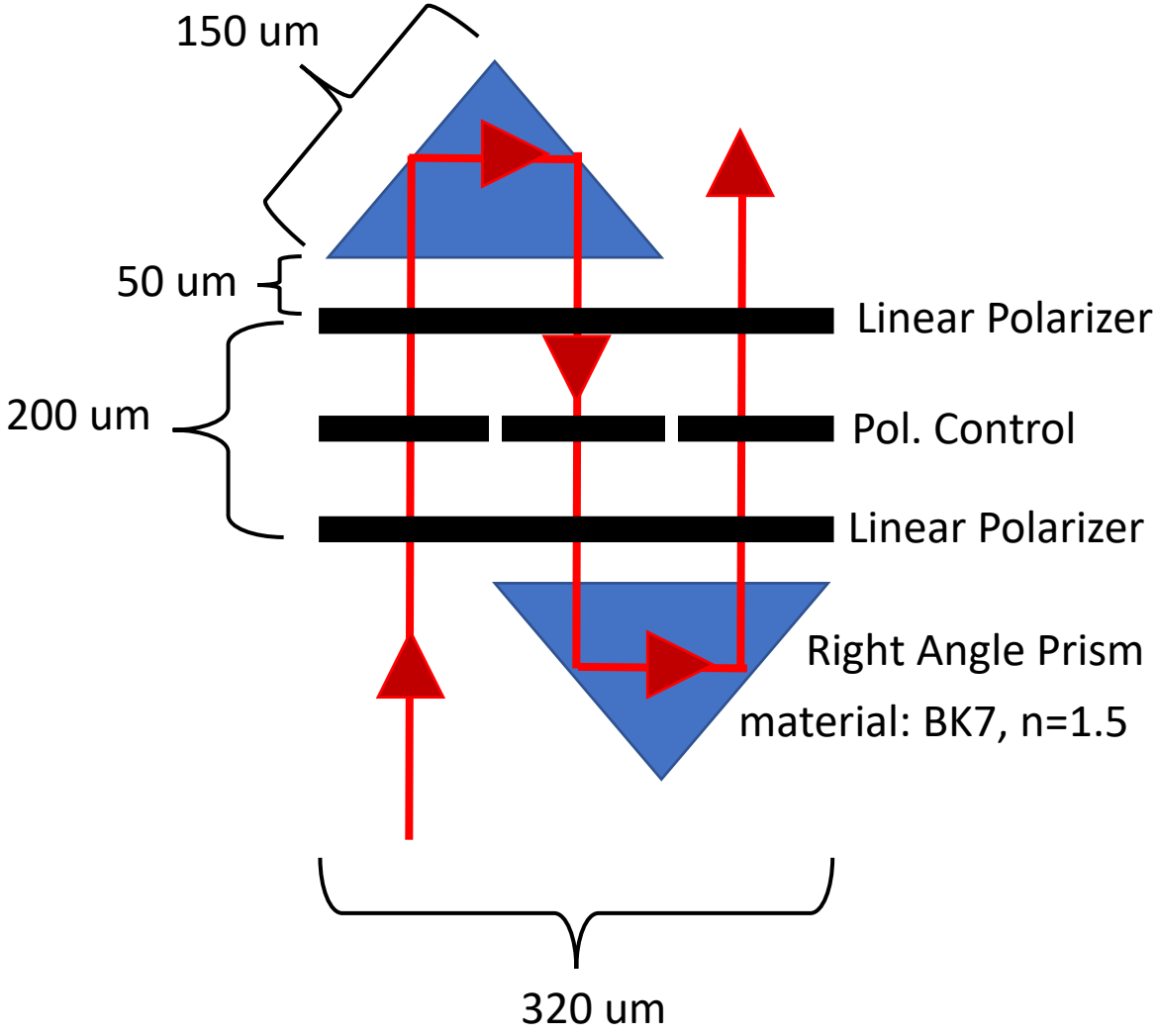
UNIVERSITA' di Pavia - Rebel Dynamics

Internal Presentation - 04/02/2022

Ray Optics Simulations (using COMSOL)

A.E. Kaplan, C. Lacava, P. Minzioni, I. Cristiani

Simulated Structure (not to scale)



Main characteristics of the simulations

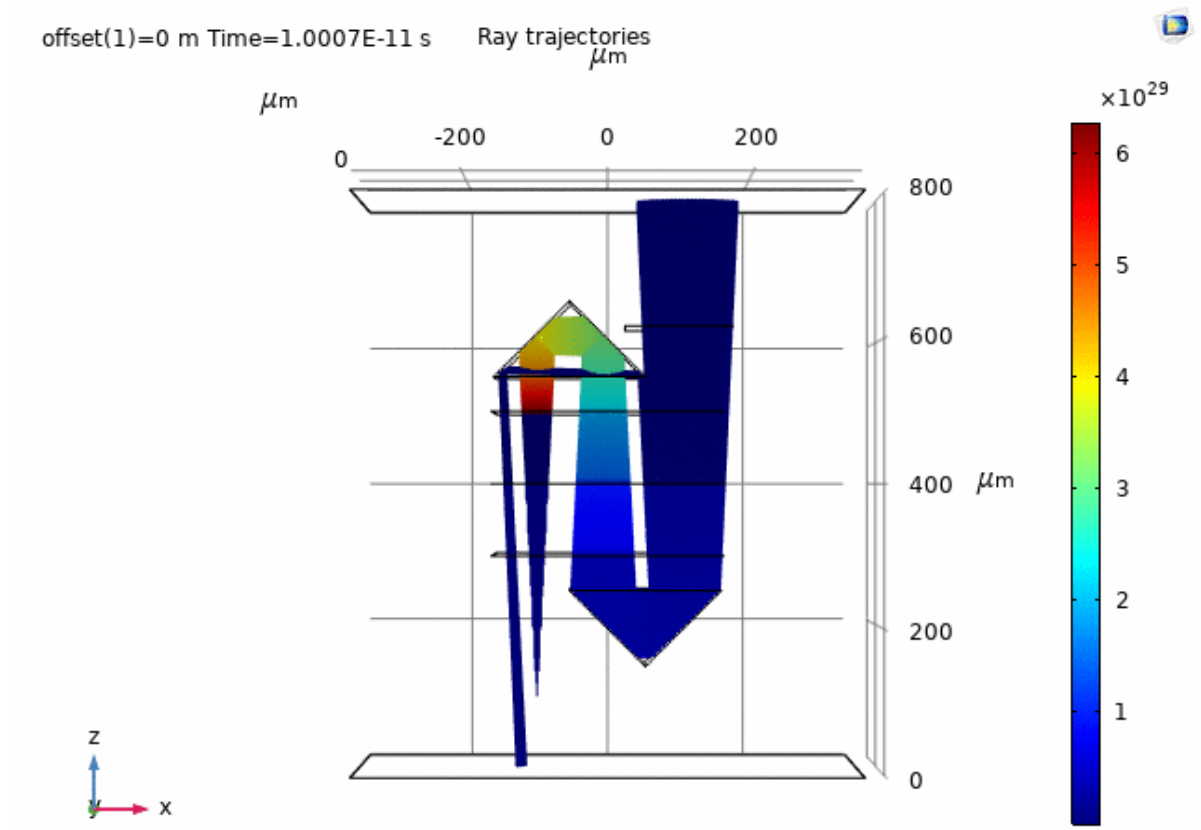
- Commercial software: COMSOL
- Ray-tracing method

Studied parameters

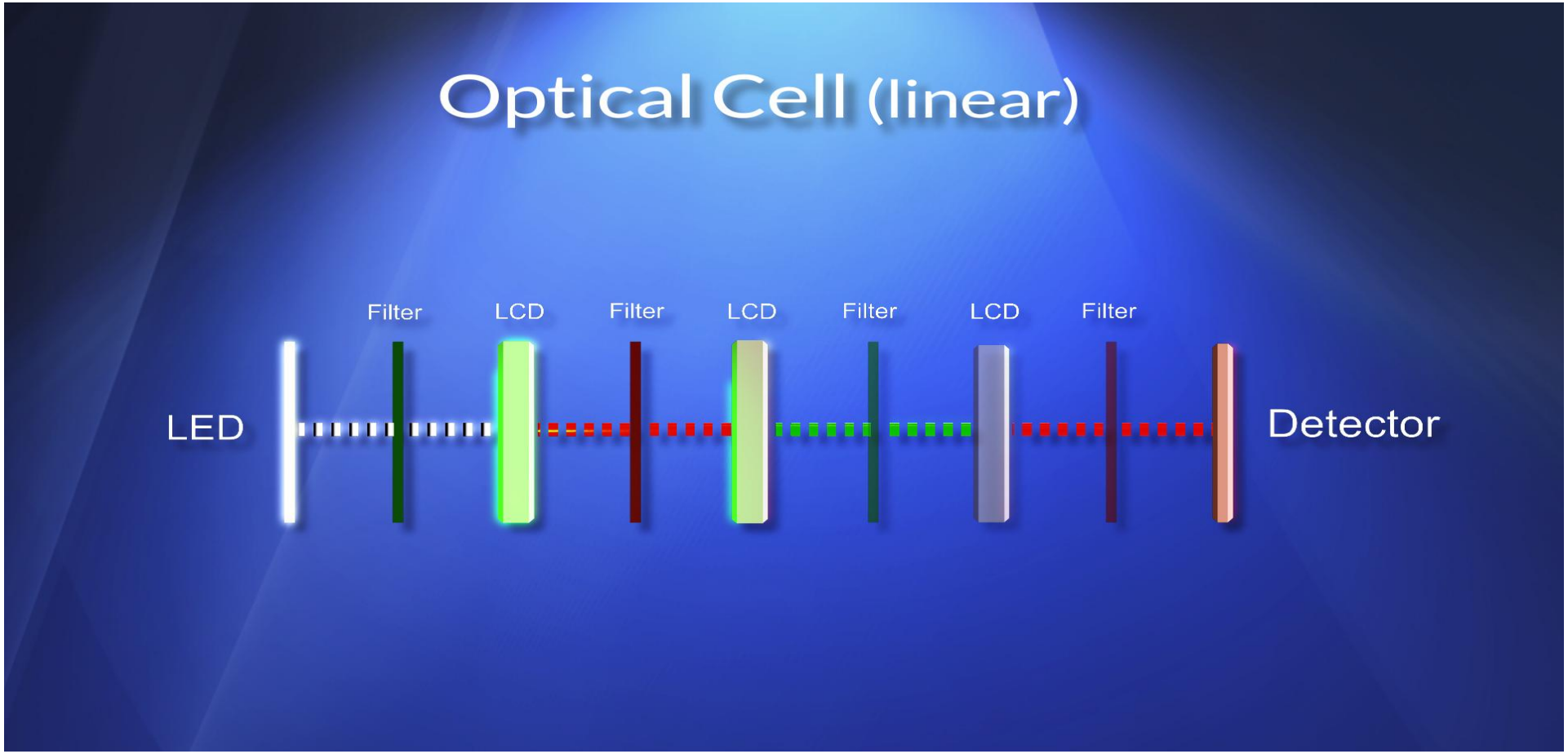
- Emission angle of the source
- Refractive index of material (prisms)
- Position of the prisms

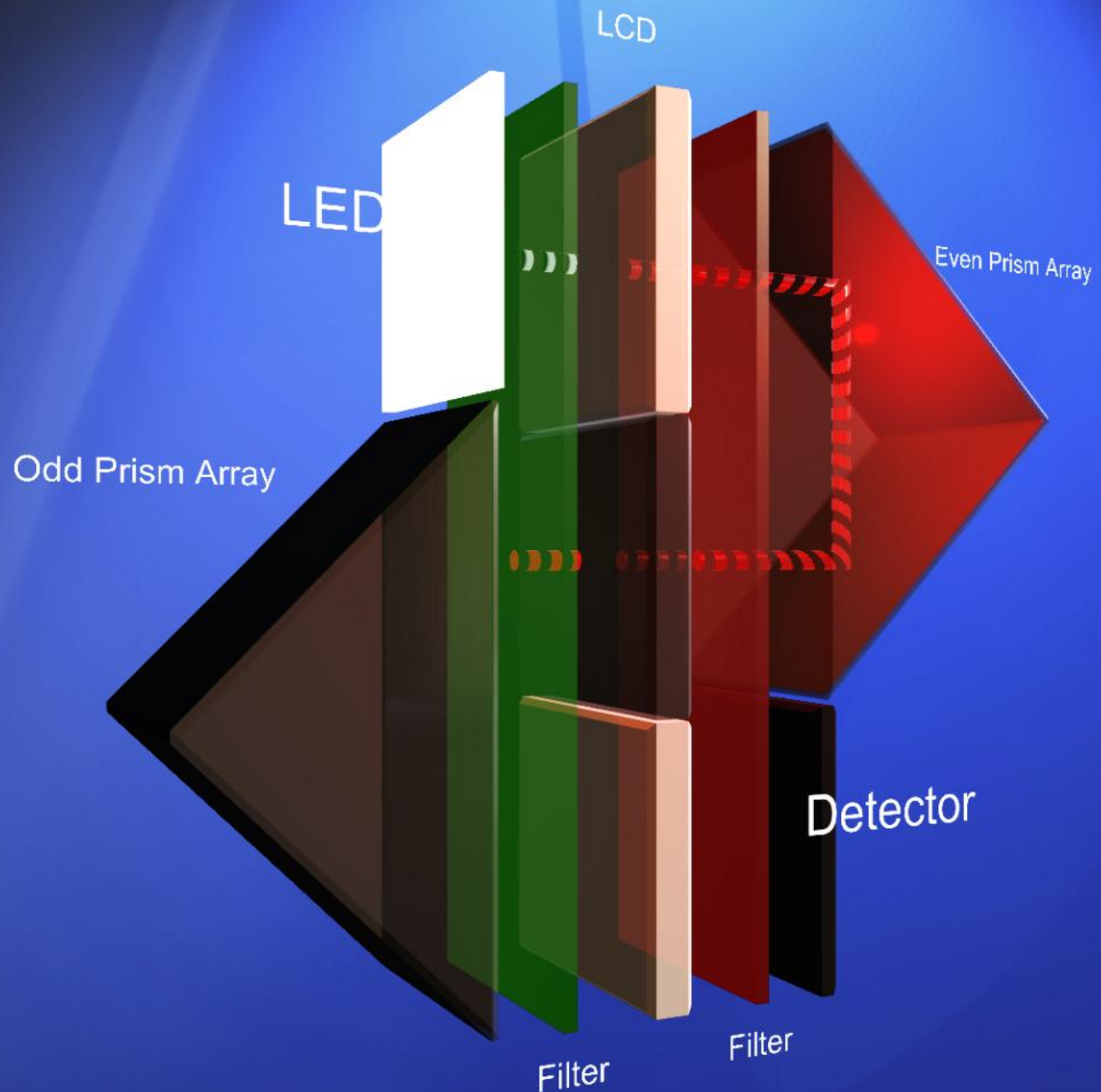
Results – Offset

According to the simulation results, offset = 0 seems to be a design rule if the angle is not sufficiently small.

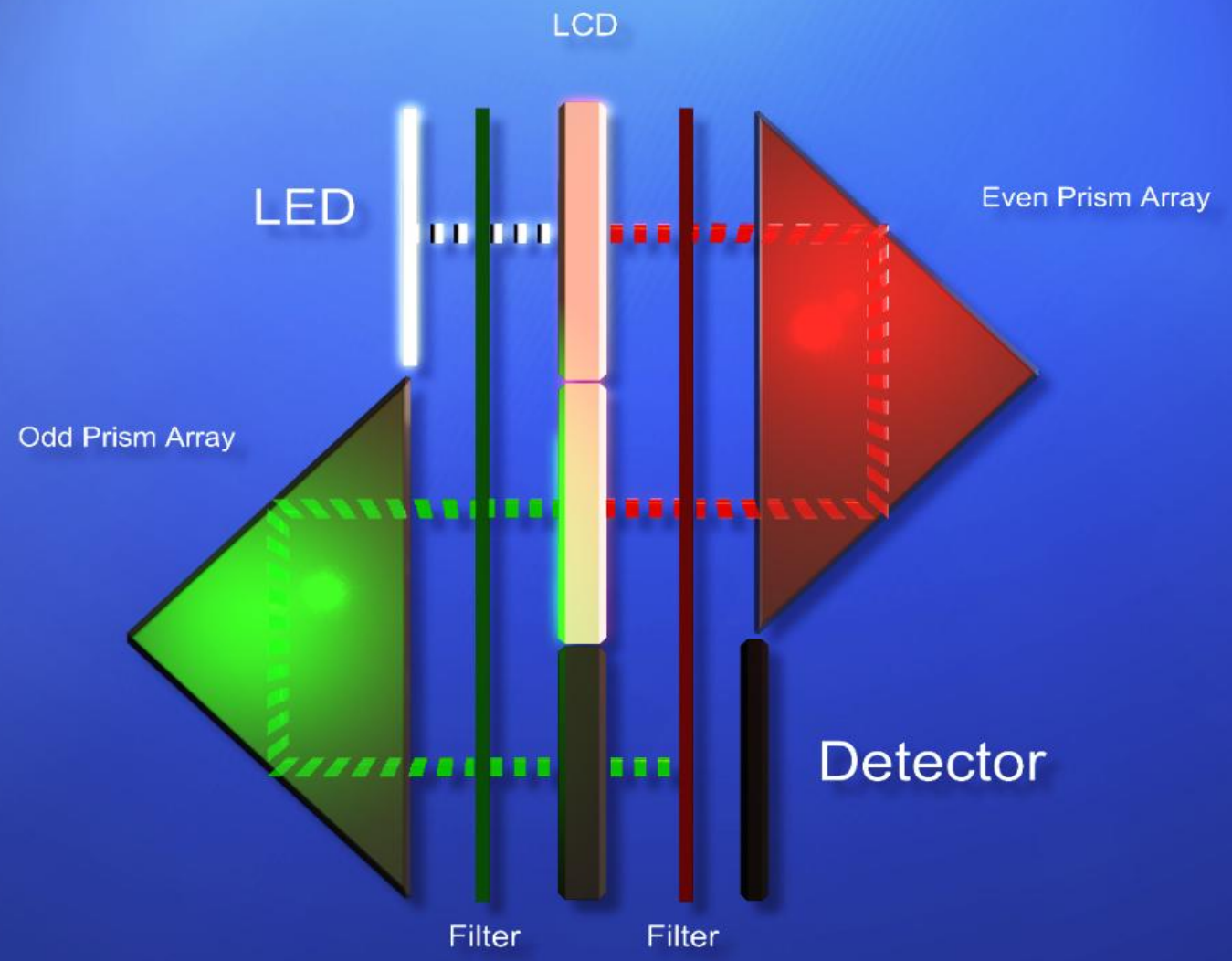


Photonic Processor cell operation



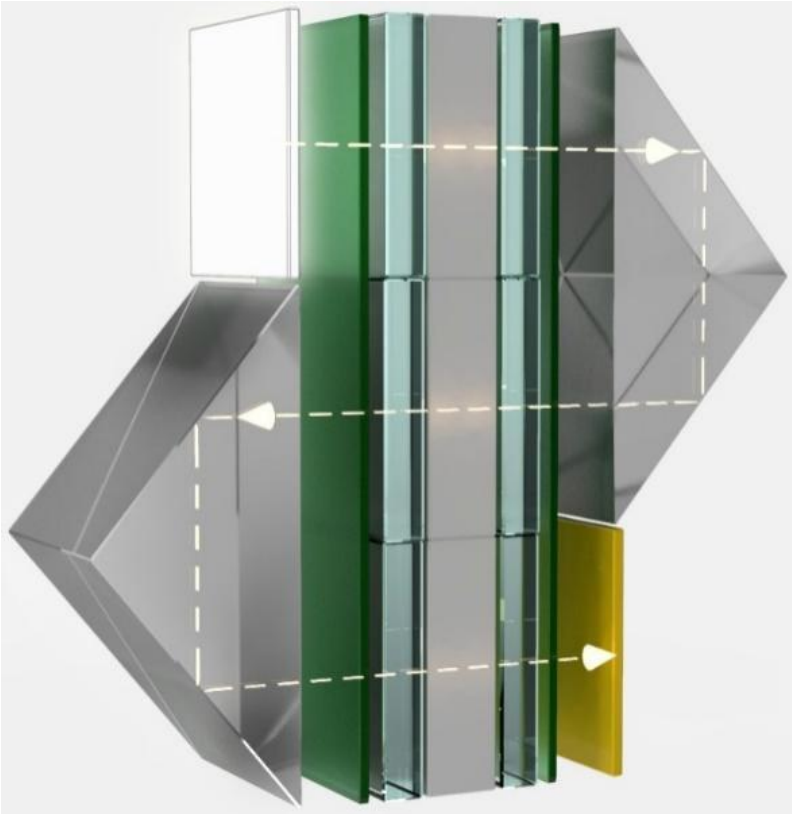

LCD
LED
Even Prism Array
Odd Prism Array
Detector
Filter
Filter

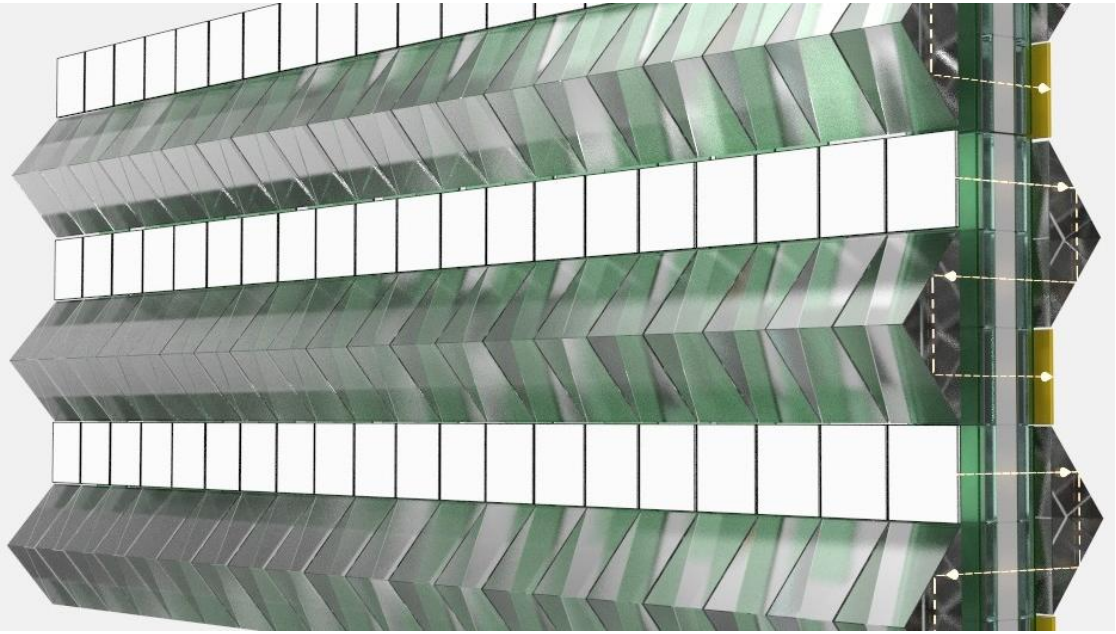
Optical Cell (optimized)



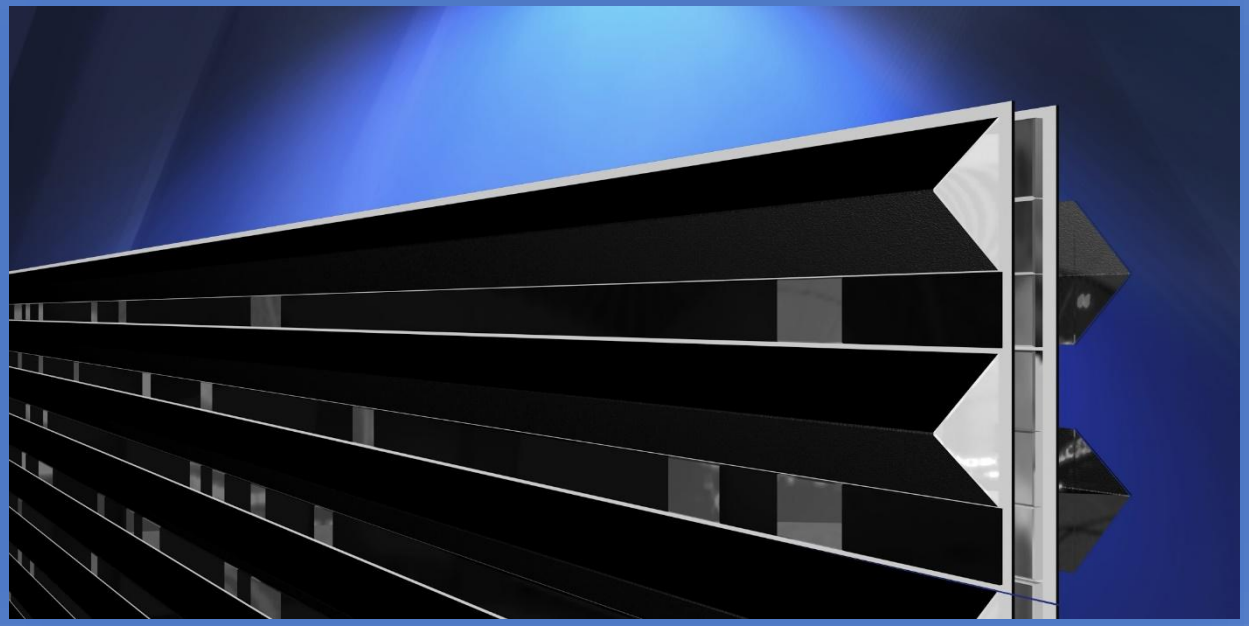
System structure

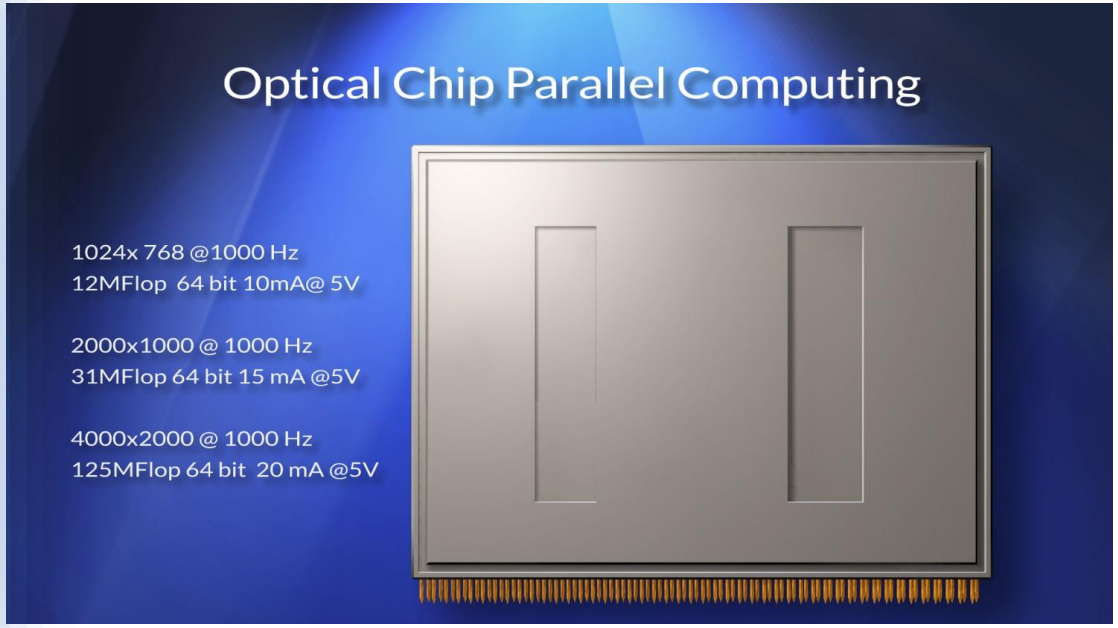
Photonic Processor single element and matrix



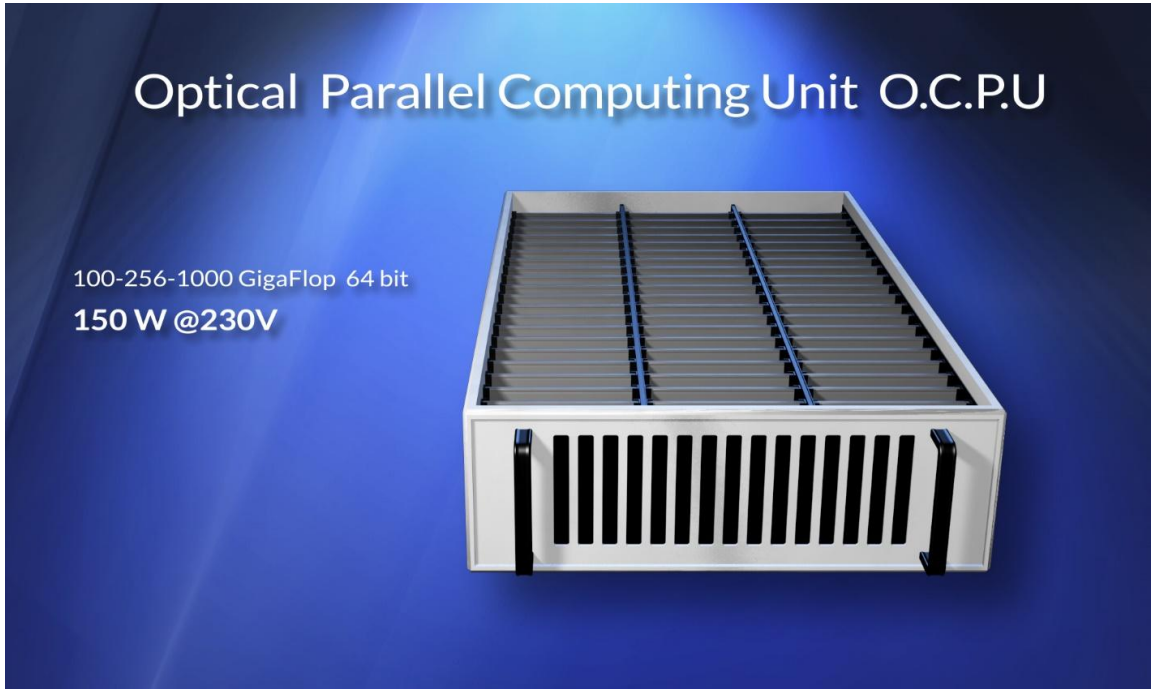


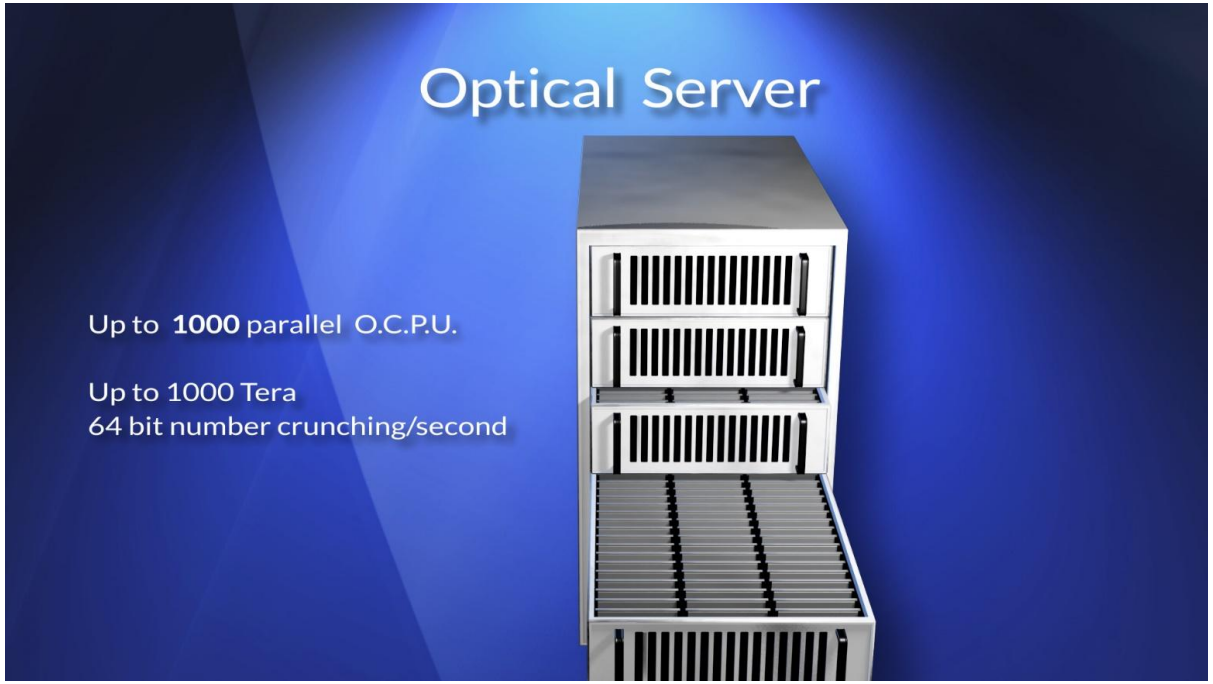
Hardware solutions





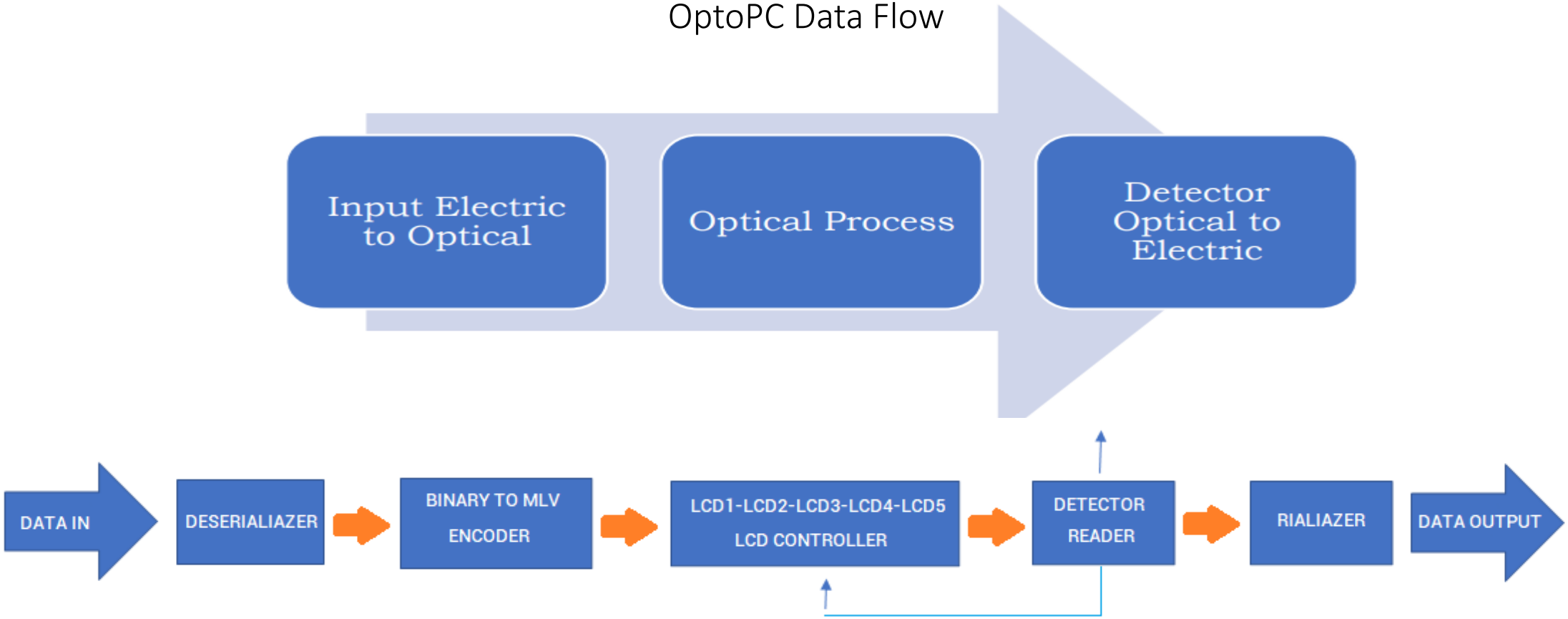
Hardware solutions

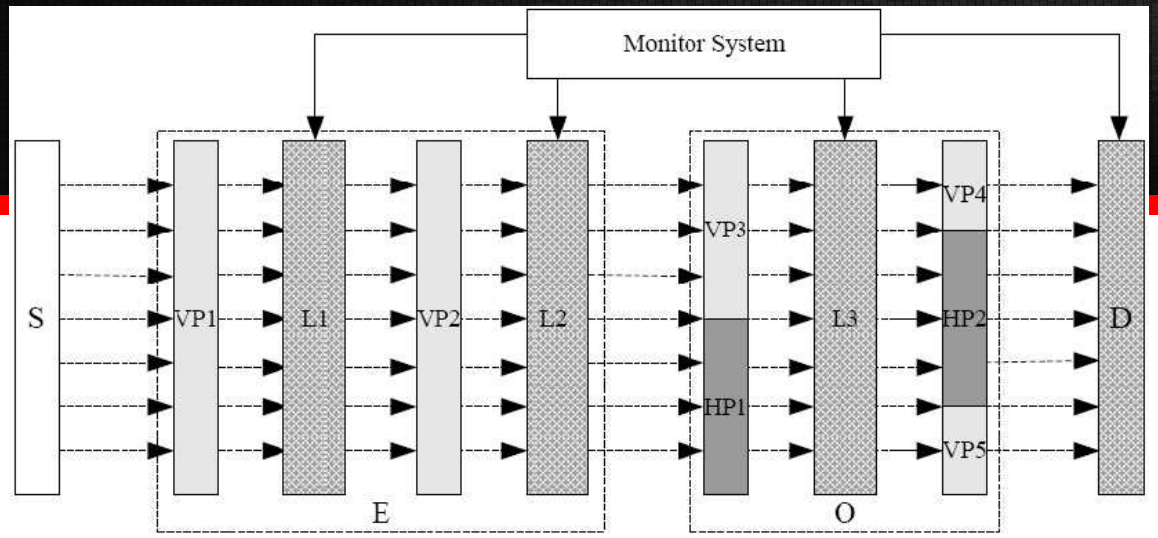




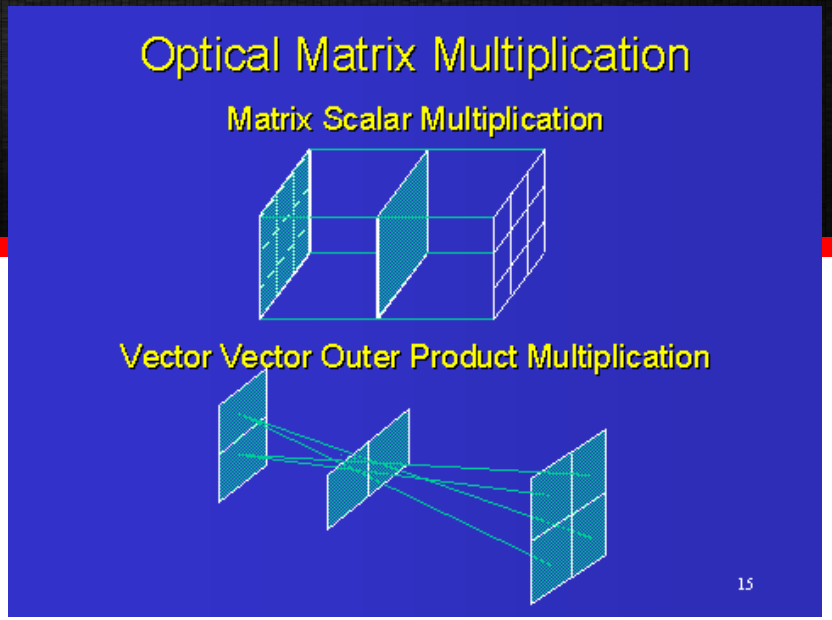
data processing

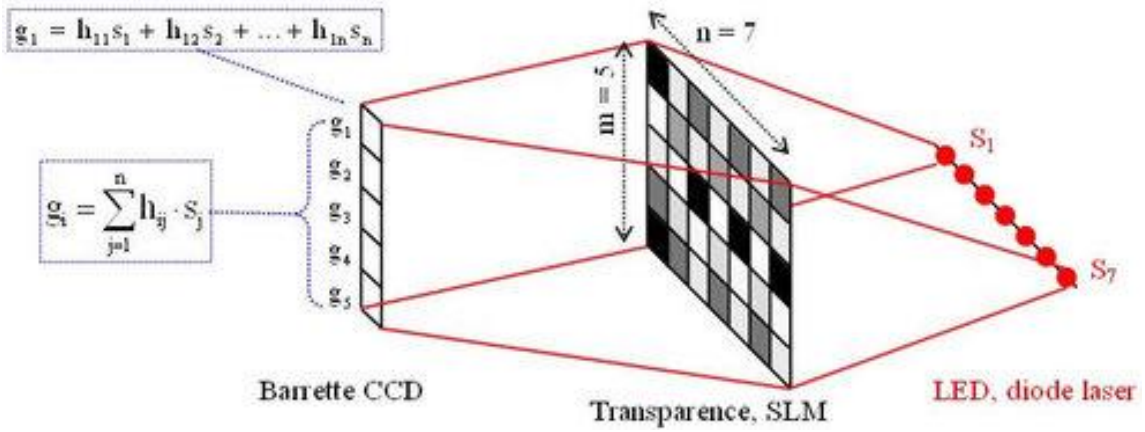
OptoPC Data Flow

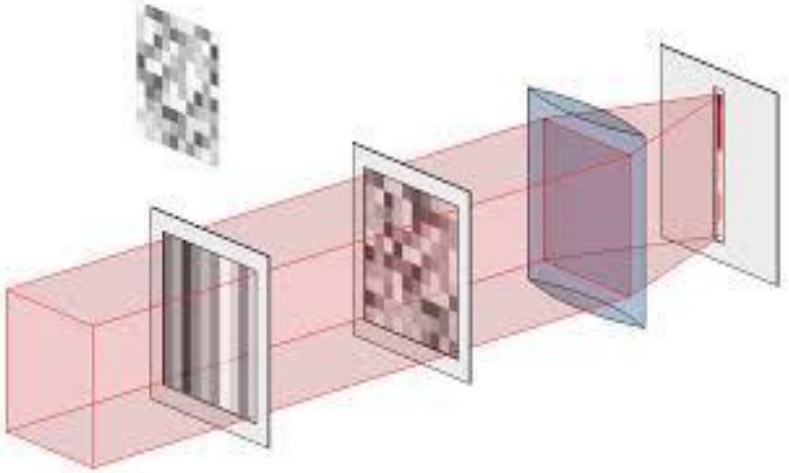



Monitor System
S
VP1
L1
VP2
L2
VP3
HP1
L3
VP4
HP2
VP5
D
E
O

*


Optical Matrix Multiplication
Matrix Scalar Multiplication
Vector Vector Outer Product Multiplication
15

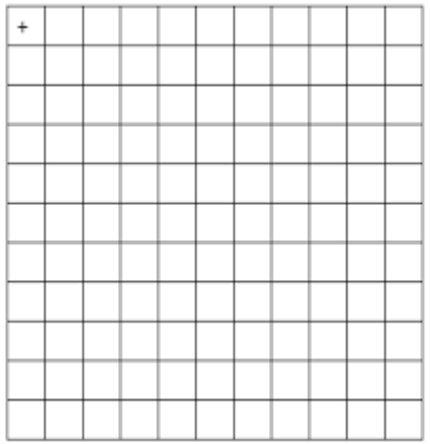

$g_1 = h_{11}s_1 + h_{12}s_2 + \ldots + h_{1n}s_n$
$g_i = \sum_{j=1}^{n} h_{ij} \cdot s_j$
n = 7
m = 5
S_1
S_7
Barrette CCD
Transparence, SLM
LED, diode laser

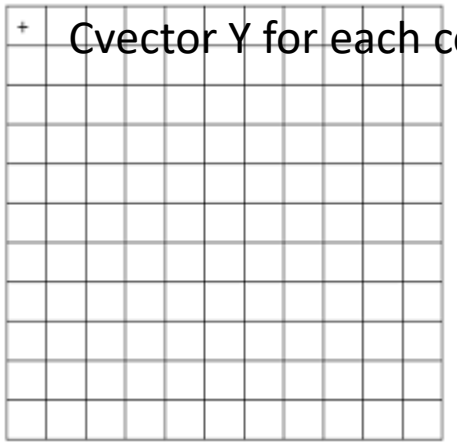


Vector by Matrix multiply

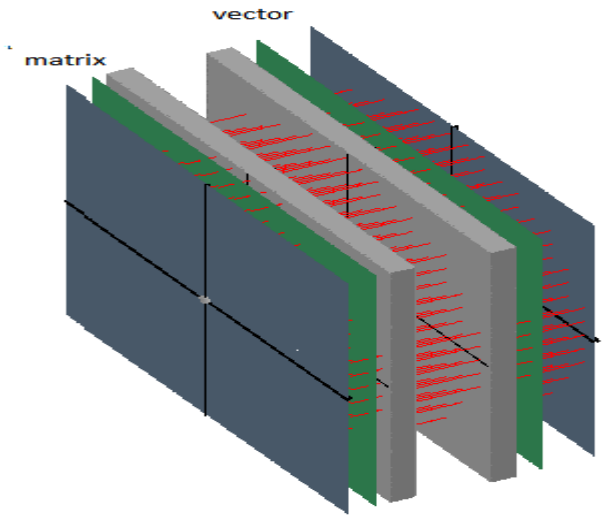
Matrix A

$$\mathbf{A} \cdot \vec{X} = \vec{Y} = \begin{bmatrix} a_{11} & \cdots & a_{1n} \\ \vdots & \ddots & \vdots \\ a_{m1} & \cdots & a_{mn} \end{bmatrix} \cdot \begin{pmatrix} x_1 \\ \vdots \\ x_n \end{pmatrix} = \begin{pmatrix} y_1 \\ \vdots \\ y_m \end{pmatrix}$$



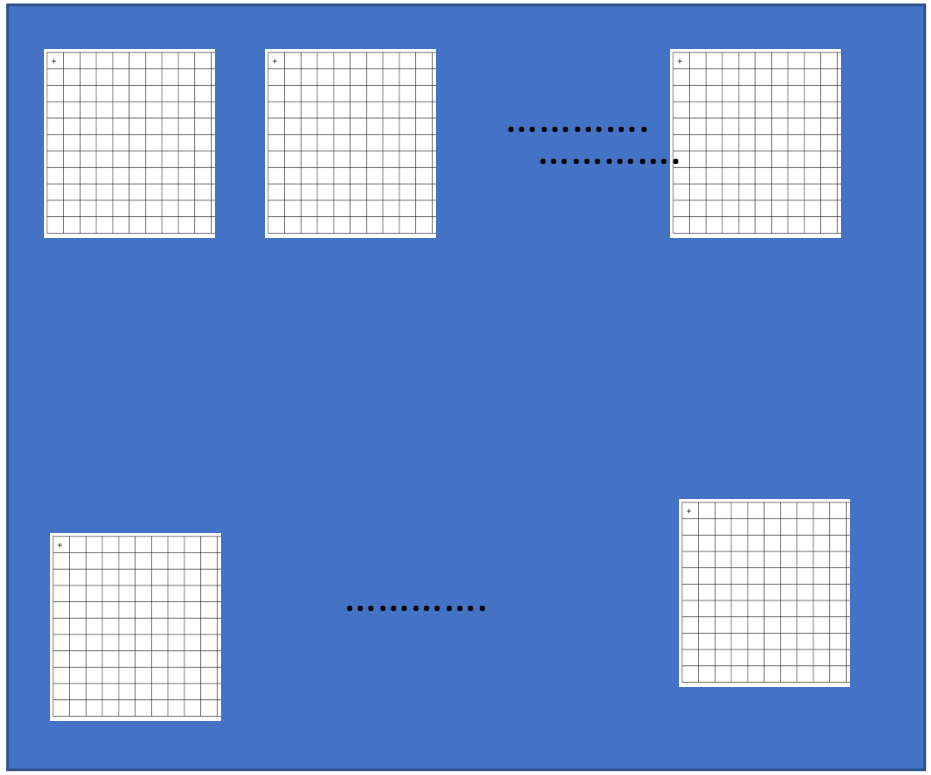


Cvector Y for each column

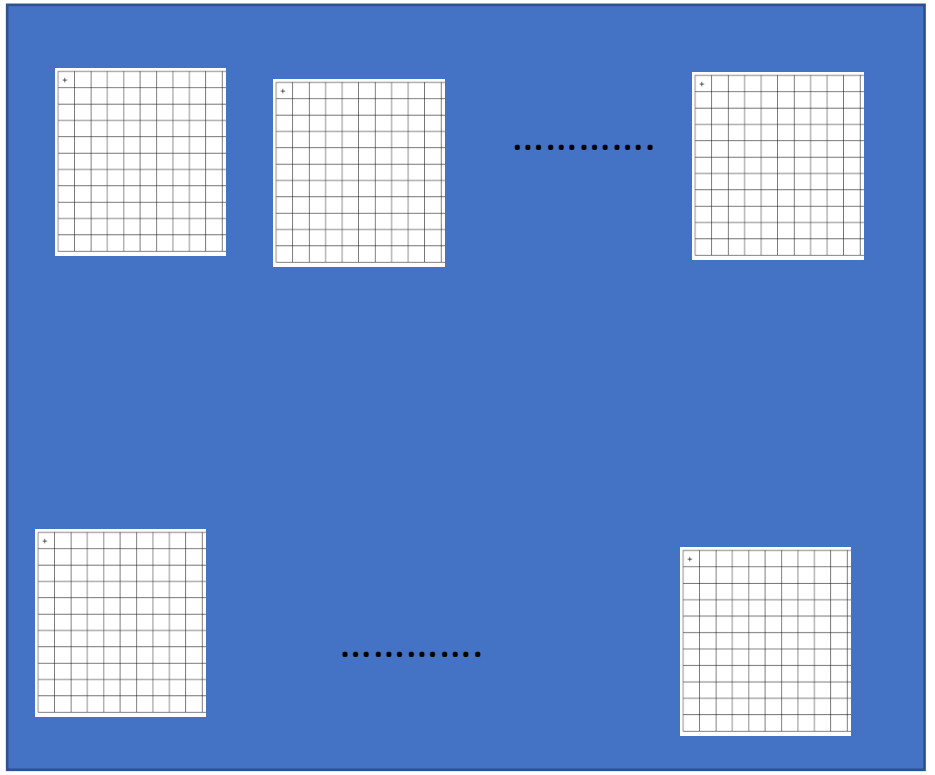


Ex. one step100x100 matrix multiply on a 1000x1000 LCD

1° LCD 1000 x 1000 write 100 matrix



2LCD matrix 1° colum…….matrix nth column

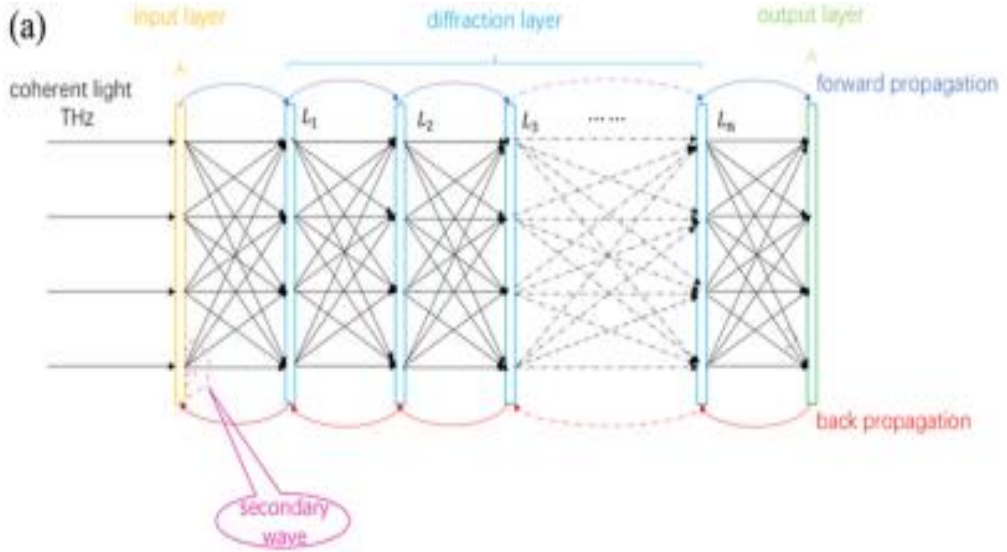


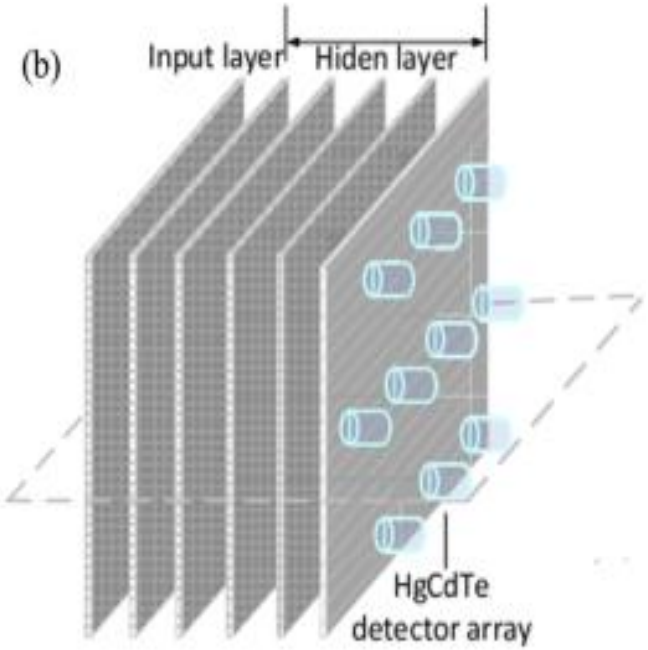
Algorith it’s only the way to write data into the LCD cell, just like to write an image om LCD

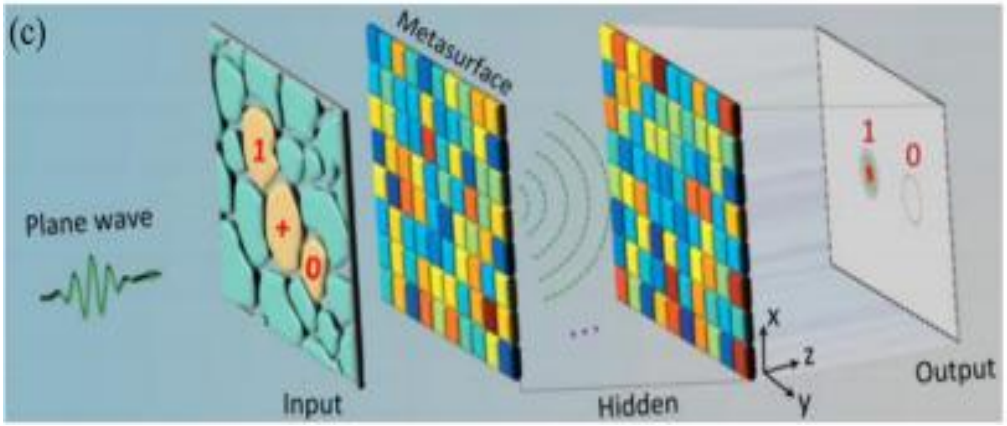
Sone numbers

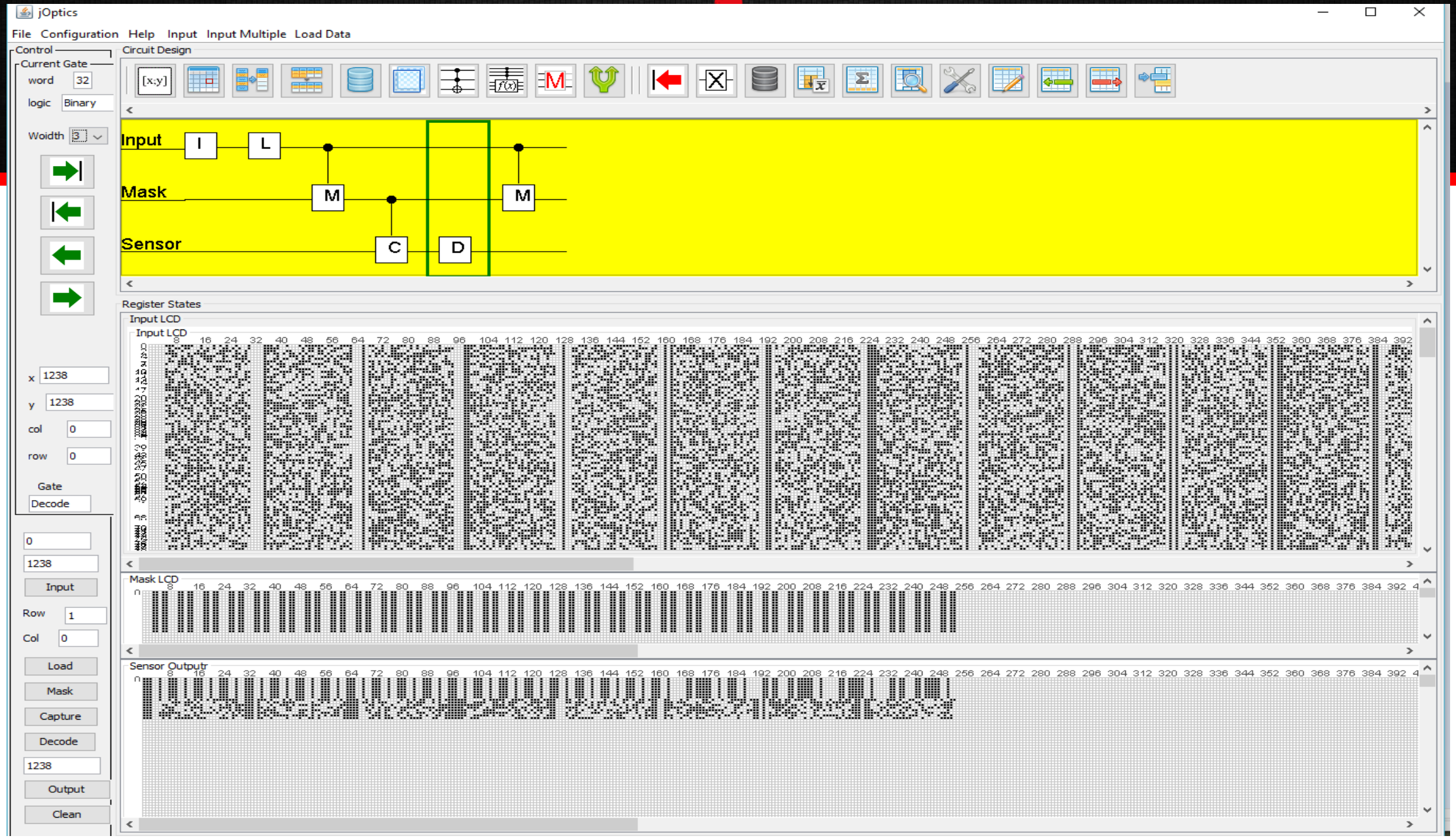
- LCD can have up to 2000 x 2000 pixels
- Can switch at 500 Hz
- Computing mulyiply of 2 Matrix 100x100 needs 10.000mulyipplcation and 10.000 sum
- LCD matrix multiplication can be done im 1 step and tajes 2ms
- Thousands of optical chip (LCD) can be parallelized
- An optical chip use less than 100 mW

*

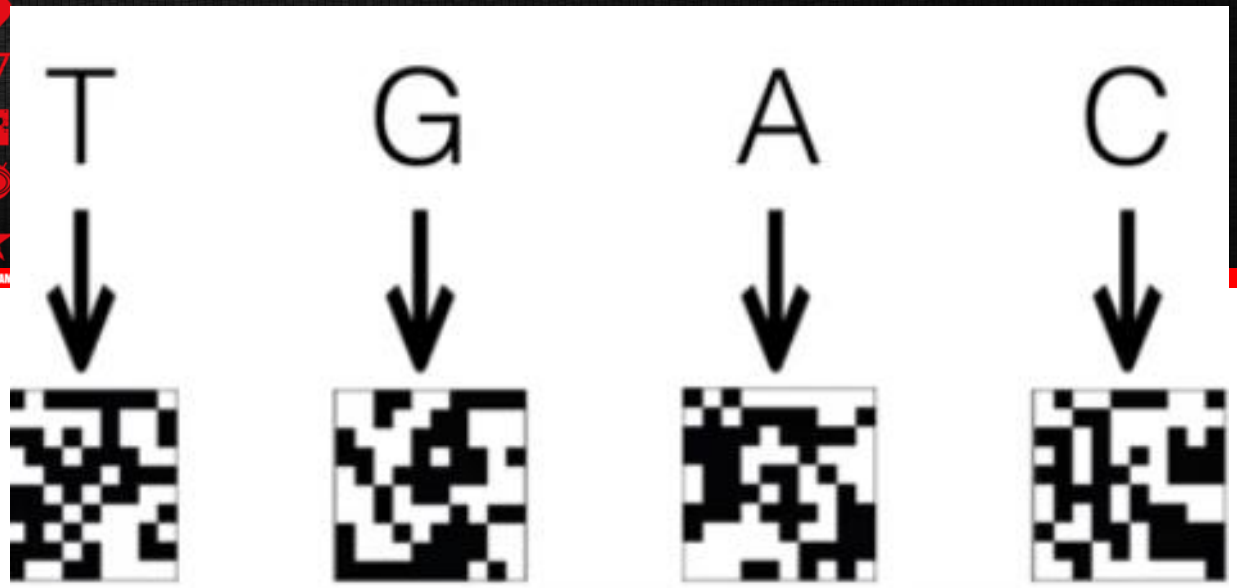

(a)
input layer
diffraction layer
output layer
coherent light
THz
forward propagation
back propagation
secondary wave


(b)
Input layer
Hiden layer
HgCdTe
detector array

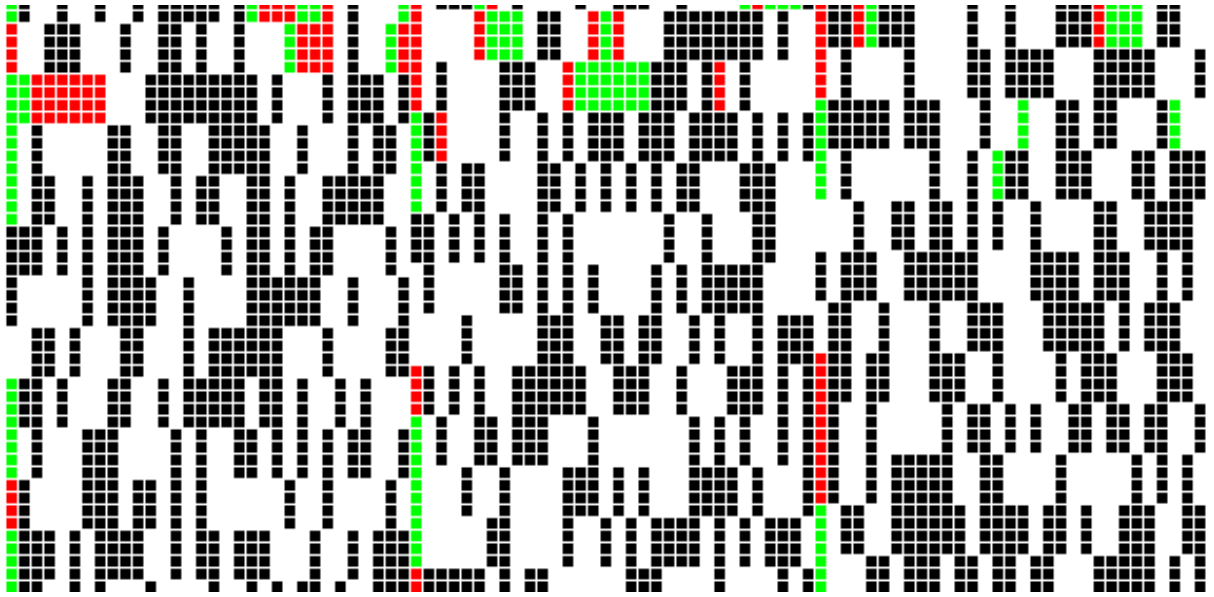

(c)
Metasurface
Plane wave
Input
Hidden
Output

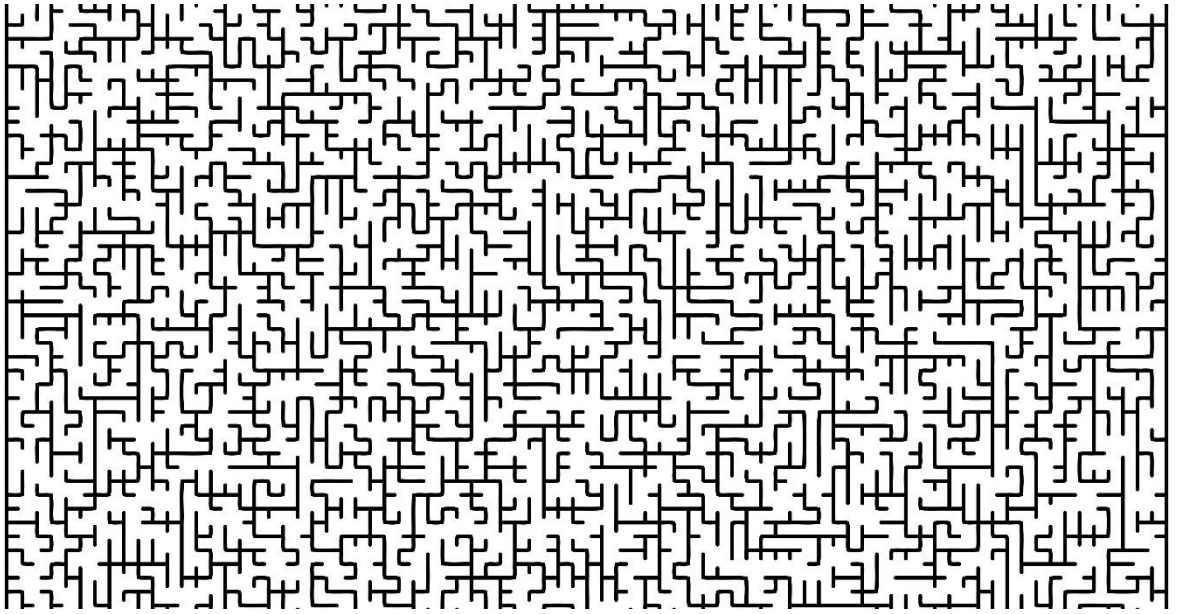

jOptics
File Configuration Help Input Input Multiple Load Data
Control
Current Gate
word 32
logic Binary
Woidth 3
x 1238
y 1238
col 0
row 0
Gate
Decode
0
1238
Input
Row 1
Col 0
Load
Mask
Capture
Decode
1238
Output
Clean
Circuit Design
Input
Mask
Sensor
I
L
M
M
C
D
Register States
Input LCD
Mask LCD
Sensor Outputr




T
G
A
C

*





Kuwait J. Sci. Eng. **31**(2) pp. 189-202, 2004

Parallel high-radix negabinary signed-digit arithmetic operations: one-step trinary and one-step quaternary addition algorithms

H. A. KAMAL

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P.O.Box 5969; Safat 13060; Kuwait. Fax: (965) 481-7451;
Email: hakamal@eng.kuniv.edu.kw

ABSTRACT

More efficient one-step negabinary signed-digit algorithms for the addition/subtraction operations are proposed. To increase the information storage density high-radix (trinary with radix = -3 and quaternary with radix = -4) negabinary signed-digits are employed. It is shown that by using digits grouping of the negabinary signed-digits, a huge reduction of the number of the symbolic substitution computation rules involved in the arithmetic computations will be achieved. The proposed algorithms are very suitable for optoelectronic implementation where various holographic and nonholographic methods based on symbolic substitution content addressable memory (CAM) can be employed. Among them, the method of joint spatial encoding technique and an incoherent optical correlator to act as a shared CAM will be presented.

Keywords: high-radix arithmetic; negabinary signed-digit; Optical computing; parallel algorithms; symbolic substitution.

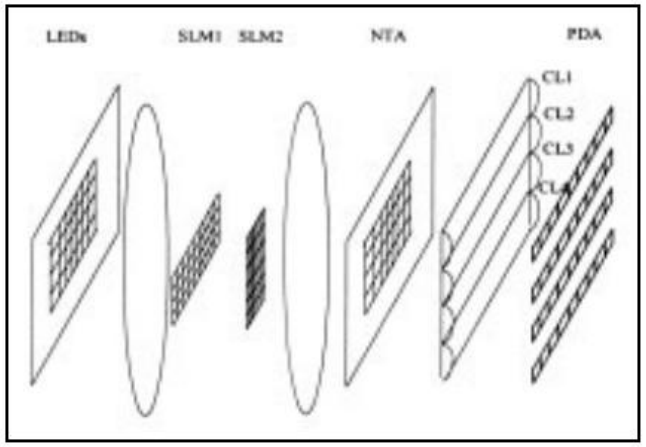


Fig. 3. Incoherent optical correlator processor to implement the NSD arithmetic (After reference 11). LED, light emitting diodes; SLM, spatial light modulator; NTA, nonlinear thresholding array; CLs, cylindrical lens arrays; and PDA, photodetector array.

NLOP's digits group for the NQSD numbers.

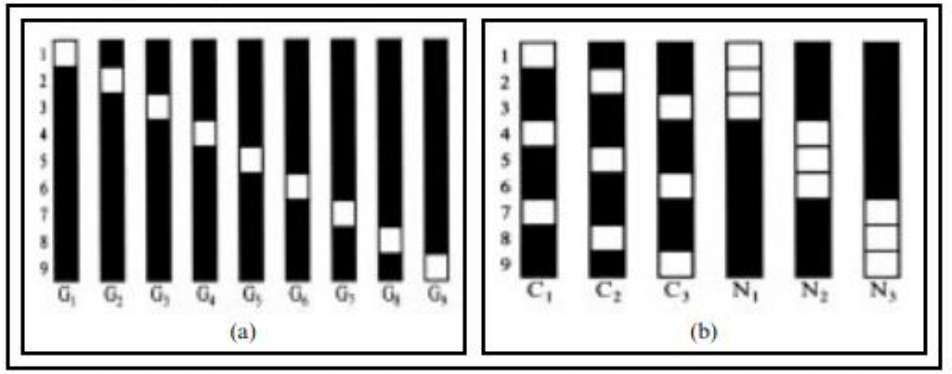


Fig. 1. (a) 9-pixels joint spatial encodings for the 9×1 pixels for the NTSD. G_1, G_2, G_3,... represent the digit groups numbers and **(b)** the new CP's and NLOP's group classifications of input digits representing the 9-pixel encodings for the NTSD adder.

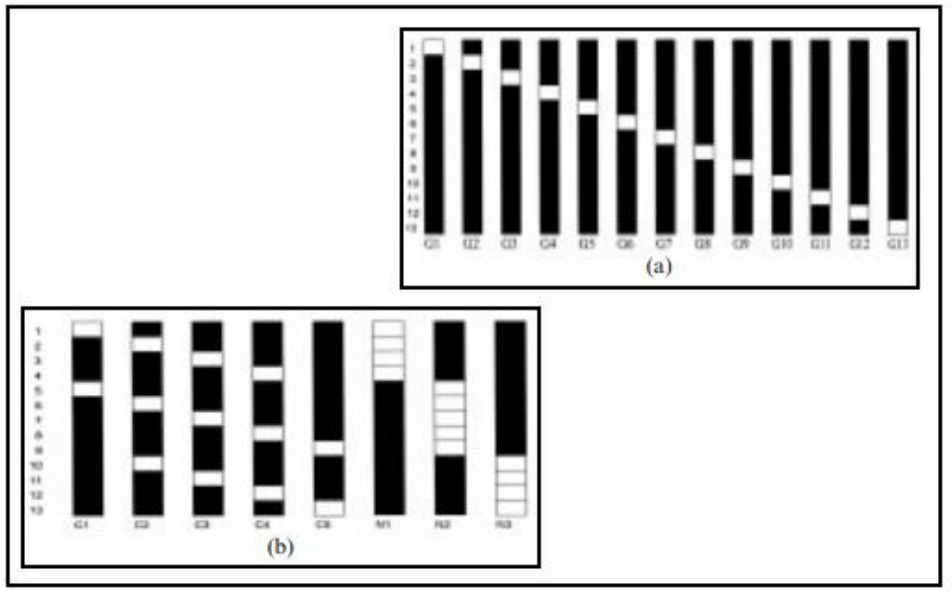


Fig. 2. (a) 13-pixels joint spatial encodings for the 13×1 pixels for the NTSD. G_1, G_2, G_3,... represent the digit groups numbers and **(b)** the new CP's and NLOP's group classifications of input digits representing the 13-pixel encodings for the NQSD adder.

*

SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

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doi: 10.1007/s11432-012-4668-6

Principle of a one-step MSD adder for a ternary optical computer

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School of Computer Engineering and Science, High Performance Computing Center, Shanghai University, Shanghai 200072, China

Received September 2, 2012; accepted December 17, 2012; published online January 31, 2013

Abstract While investigating a three-step MSD adder and the reliability thereof for ternary optical computers (TOC), the principle of one-step MSD addition was found. An important concept, the mid-bit transform, is proposed. Next, the important mid-bit transform table (MTT) for 3-bit MSD input and the corresponding mid-bit transform unit (MTU) are obtained. Using the principle, the concept structure of a one-step MSD adder is proposed such that the sum of the addition can be obtained easily in one step in parallel. By restricting the input symbols, a simplified MTT is obtained and the principle of a one-step adder with restricted input symbols is introduced, together with the corresponding simplified concept structure of a one-step MSD adder. Two examples are presented to demonstrate the principles of one-step MSD adders. This work lays the theoretic foundation for the design of an optical MSD adder in future study.

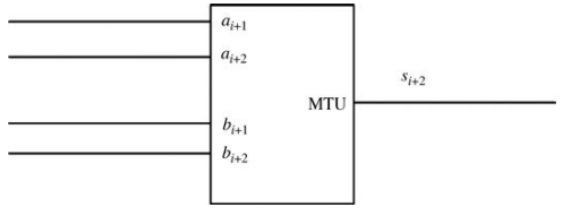


Figure 3 Mid-bit transform unit with restricted input symbols.

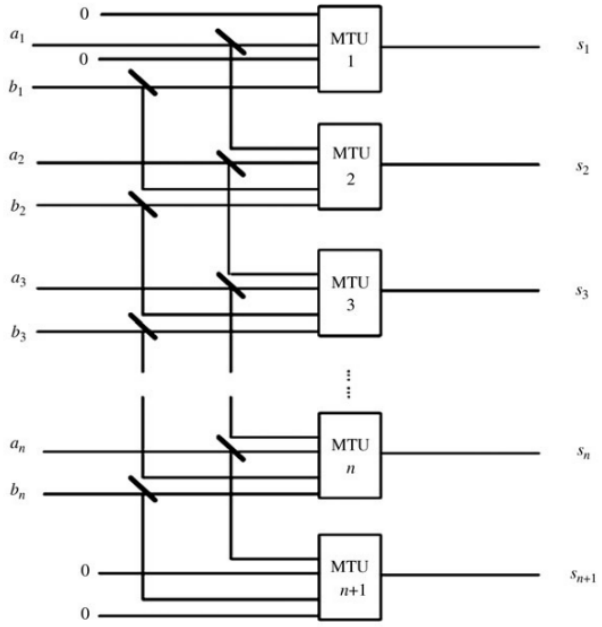


Figure 4 Mid-bit transform unit with restricted input symbols.

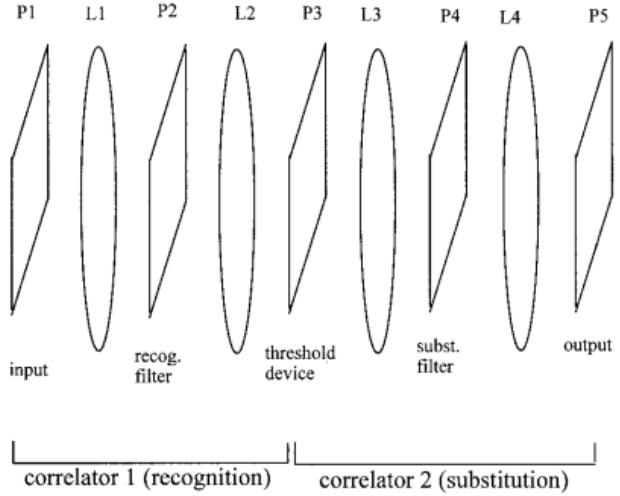
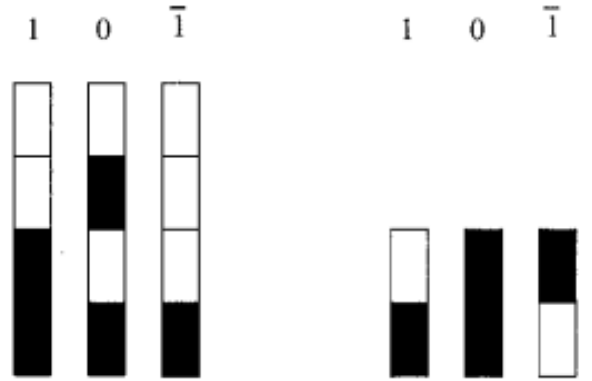
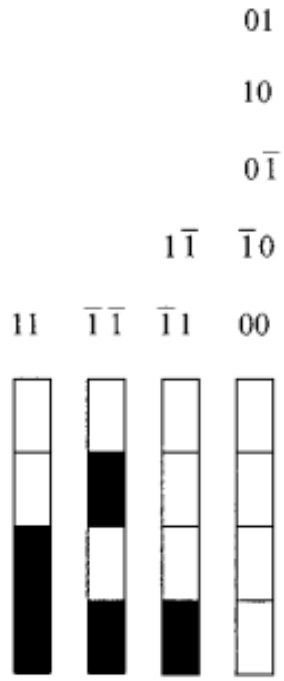


Fig. 1. Basic symbolic substitution cascaded correlator architecture after Ref. 17.

*





Algorithms for optoelectronic implementation of modified signed-digit division, square-root, logarithmic, and exponential functions

Abdallah K. Cherri and Mohammad S. Alam

Algorithms for computing complex elementary functions based on the modified signed-digit (MSD) number system representations are proposed. An arithmetic unit that performs parallel one-step addition (subtraction), multiplication, and division is proposed to achieve the computation of complex functions such as the square-root, logarithm, exponential, and other related operations. An optoelectronic correlator-based architecture is suggested for implementing the proposed MSD algorithms to compute the above-mentioned elementary functions. We utilized the symbolic substitution technique to reduce the number of computation rules involved. © 2001 Optical Society of America

OCIS code: 200.0200.

ELSEVIER

Optics & Laser Technology

Optics & Laser Technology 30 (1998) 515–525

Parallel quaternary signed-digit arithmetic operations: addition, subtraction, multiplication and division

Mahmoud K. Habib*, Abdallah K. Cherri

Department of Electrical and Computer Engineering, College of Engineering and Petroleum, Kuwait University, P.O. Box 5969, Safat 13060, Kuwait

Received 30 November 1998; accepted 14 January 1999

Abstract

A quaternary signed-digit number representations-based arithmetic unit is proposed. The arithmetic unit performs parallel one-step addition (subtraction), multiplication and division. We use the symbolic substitution technique to reduce the number of the computation rules involved in the computation rules. Fast parallel nonrecoded quaternary signed-digit multiplication is proposed using our proposed one-step quaternary signed-digit adder. Also, parallel quaternary signed-digit division is performed

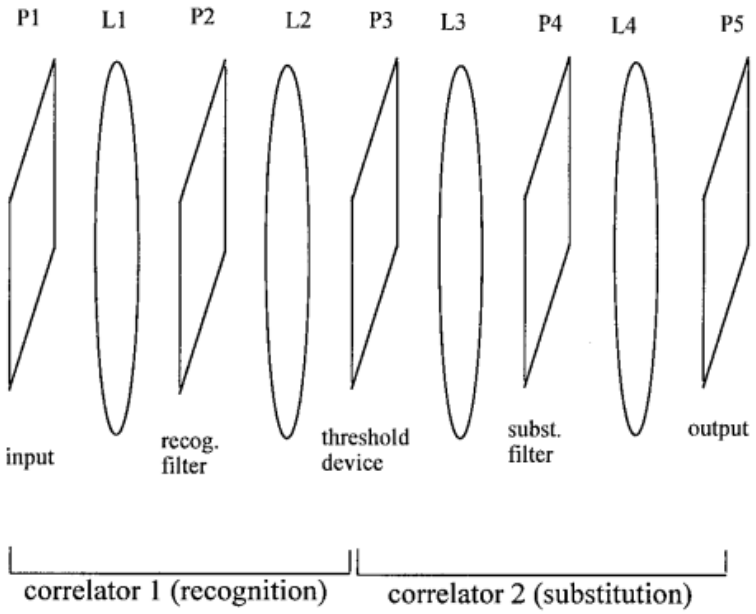


Fig. 1. Basic SS cascaded correlator architecture after Ref. [17].

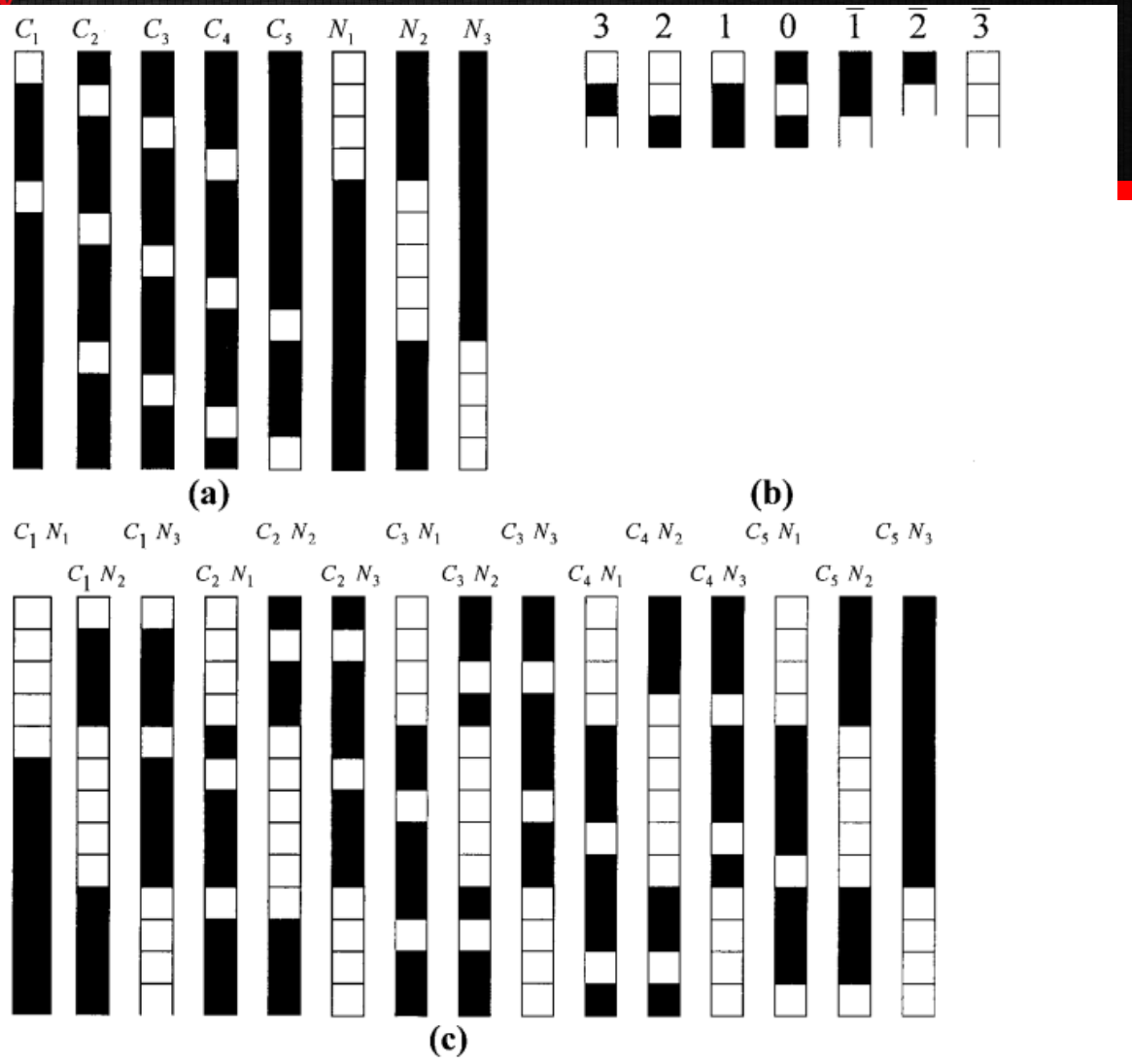


Fig. 2. One-step QSD addition: (a) 13-pixel encodings for CP and NLOP digit classes; (b) spatial encodings that are used in the inp
(c) the superimposed spatial encodings that are used in the **X** matrix.

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International Bureau

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WIPO | PCT

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

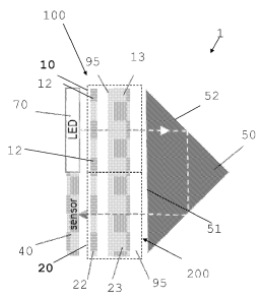
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*
— *in black and white; the international application as filed contained color or greyscale and is available for download from PATENTSCOPE*

(54) **Title:** PARALLEL OPTICAL COMPUTING SYSTEM

(57) **Abstract:** A parallel optical computing system is described, said system comprising: at least one first module (10) comprising at least one polarization filter (12) and at least one liquid crystal cell (13), the first module (10) being configured as an optical modulator (100) for receiving light from a light source (70) and for encoding the light output from the liquid crystal cell (13) into optical data to be processed; at least one second module (20) comprising at least one polarization filter (22) and at least one liquid crystal cell (23), the second module (20) being able to be configured as an optical processor (200) for receiving the optical data to be processed and for outputting an optical result of the processing; at least one optical detector (40), designed to receive the optical result of the processing and convert the optical result into a corresponding electrical result.

Fig. 1



WO 2021/205213 A1

*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/IB2020/053388

6. ☒ With regard to top-up searches (Rules 66.1 *ter* and 70.2(f)):
   ☒ A top-up search was carried out by this Authority on 06.01.2022 (all discovered documents are listed in the Supplemental Box Relating to Top-up Search).
   ☐ Additional relevant documents have been discovered during the top-up search.
   ☐ No top-up search was carried out by this Authority because it would serve no useful purpose.

7. ☐ Supplementary international search report(s) from Authority(ies) has/have been received and taken into account in establishing this report (Rule 45bis.8(b) and (c)).

* *If item 4 applies, some or all of those sheets may be marked "superseded".*

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-8
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-8
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-8
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Companies involved

The Partners

main company:

OPTOPC SA - Switzerland

exclusive contractor company
to OPTOPC technology development:

REBEL DYNAMICS S.r.l. - Italy

REBEL DYNAMICS

(mechanical simulation system)

Modelling and simulation of mechanical systems

Design and manufacturing of simulation system

Custom-made Control System

(A.I. Artificial Intelligence)

Artificial Intelligence Projects

In cooperation with Omron, development of applications with machine controllers equipped with A.I. algorithms dedicated to industrial production

(robotics)

Applications in:

-Pick & Place

-Process Control

-Robot control

(control algorithms)

Development of control algorithms based on Delta-Tau Omron motion computer

The PMAC was used to grind the corrective lenses for the original Hubble Telescope and is currently at work on the new James Webb Space Telescope

The project team

OptoPC

- Engineers
- PHDs
- PMs
- Electronics, AI & ML expertise
- Prototype developing
- Concept of proof developing

REBEL DYNAMICS®

UNIVERSITÀ DI PAVIA

- Dep of Electrical, Computer Engineering
- Optical Network Units in Silicon Photonics
- PHDs
- Laboratory research and prototype developing

UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA

- Department of Materials Science
- Data processing
- PHDs
- Laboratory research and prototype developing

APITECH EVOLVING EASIER

- Innovation management
- Fundraising
- EU Lobbying

achieved milestones

what has been done

Technology Readiness Level (TRL)

1	Basic principles observed	2015-2019: math and physical definition
2	Technology concept formulated	2020, Apr: patent submission 2021, Jan: positive feedback from EPO
3	Experimental proof-of-concept	in progress
4	Technology validated in the lab	
5	Technology validated in relevant environment	
6	Technology demonstrated in relevant environment	
7	System prototype demonstration in operational environment	
8	System complete and qualifies	
9	Actual system proven in operational environment	

Exploration

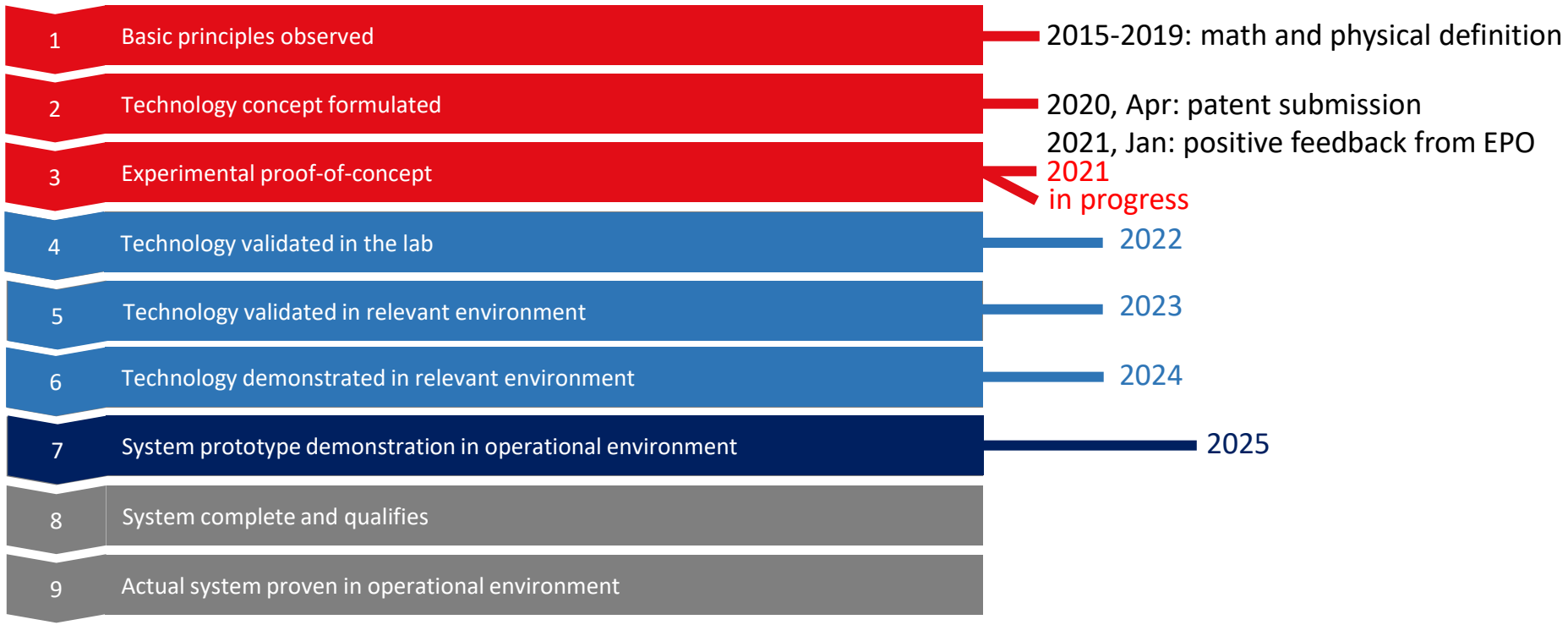
OptoPC

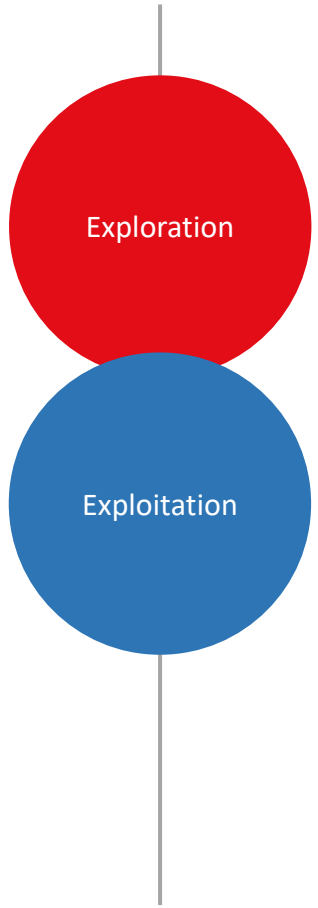
achieved milestones

4-year plan

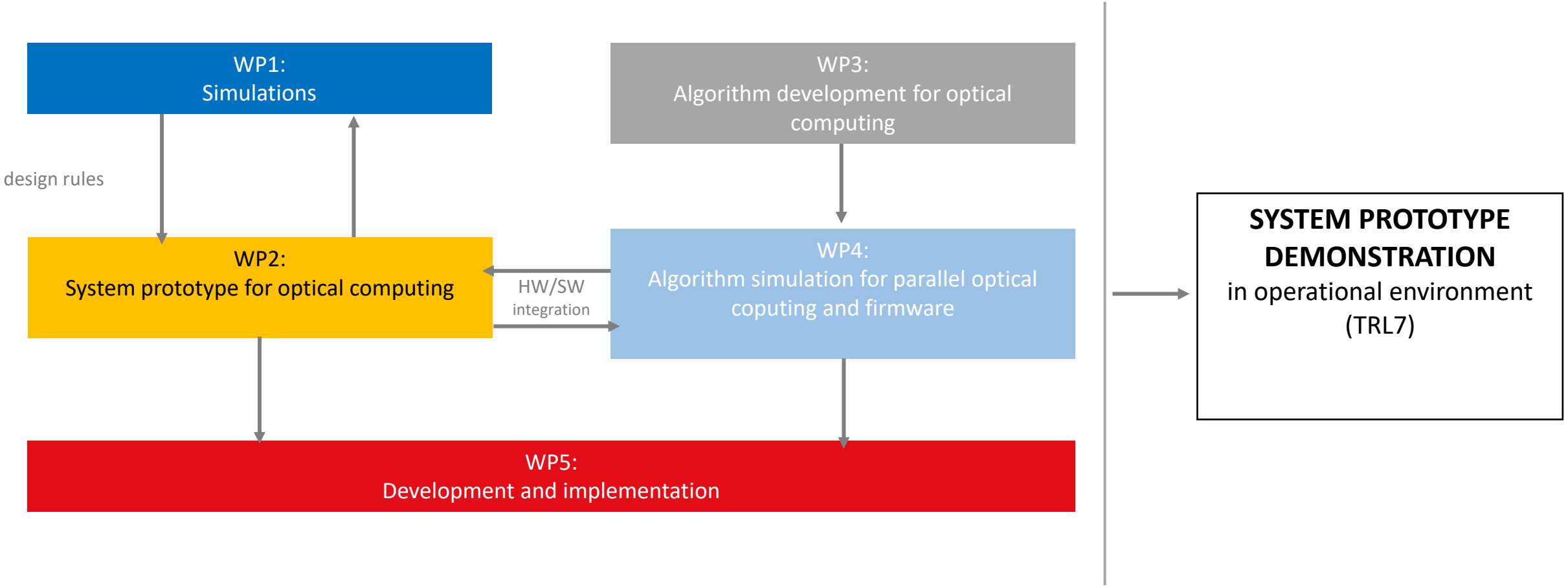
what has been done

Technology Readiness Level (TRL)





Work packages



WP1 + WP2

WP1: Simulations

1.1 Optical group simulation

1.2 Assessment of minimum light emission

1.3 Assessment of polariser filter absorption

1.4 Assessment of liquid crystal cell absorption

1.5 Assessment of prism reflectivity

1.6 Assessment of silicon sensor sensitivity minimum

1.7 Definition of device physical and mathematical model

1.8 Material identification

1.9 Technology identification

1.10 Final model

1.11 Identification of device possible manufacturer

WP2: System prototype for optical computation

2.1 Requirement definition

2.2 Literature research on equivalent systems

2.3 Lab tests with commercial LCD systems

2.4 Prototype based on an in-line system (in view of final device)

2.5 Interface fabrication to the external environment (fiber)

2.6 Definition of electronic control devices (FPGA)

2.7 Hardware design for device control

WP3 + WP4 + WP5

WP3: Algorithm development for optical computation

3.1 Literature research on existing algorithms

3.2 Algorithm fitting for new device

3.3 Definition of the optimal optical encoding

3.4 Theoretical algorithm sequences for parallel computing

3.5 Complex and sequential algorithms (vectors, matrices, database, images)

WP5: Development and implementation

5.1 Firmware application to the new device

5.2 First application with the new chip and beta testing

WP4: Algorithm simulation for parallel optical computing and firmware

4.1 Software writing for algorithm simulation

4.2 Creation of a graphical interface (JavaScript)

4.3 Simulation of data flow from and to the external environment

4.4 Algorithm application

4.5 Executing language for data and algorithms

4.6 Interface to external programs for computational activity distribution

4.7 Development of computational chains and database research

4.8 Image Analysis

CONTACTS

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